WA 9100 SERVICE NOTES 23/2 - 27/2

1. Dipswitch 7 up
   PASSWORD FOR FACTORY SELFTEST :
   7 4 1 2 5 8

2. Wanneer de ~~DIAGNOSE~~ SELFTEST wordt gebruikt kunnen de knappen FACTORY LIMITS worden geactiveerd door de softkey - rechtsboven in te drukken. Er verschijnt een kleine "f" op het scherm. De limits zijn knappen.

3. Om na inschakelen van de 9100 de SELFTEST over te slaan, moet direct na inschakelen de middelste softkey (onder het scherm) worden ingedrukt. (ca. 2 seconden).

4. A06.038 } ZEKERINGEN (boden)
   A06.039 }

5. P03.020 factory test } zekeringen.

6. Softkeys 2 en 3 (rechtsboven) voor selectie van scoopoptie-test en opt 135-test.

Dipswitches
- 6 - BOOT ENABLE
- 7 - FACTORY ENABLE
- 8 - PASS ENABLE

23/2 – 27/2 1998

WA 9100
SEPT '95 (voor deze datum).

1 ECO 4963 scoopoptie 250
2 F/W < 2.06

ECO 1762 30V range DC → bias current 240 mV wordt 300 m

ECO 4944 Wanneer selftest fail p 02.002 (before okt. '95)
remove resistor R251 (power board).

ECO 4944 Outputtransistors kunnen ander type zijn. (before sept '
weerstanden moeten veranderd worden (zie schema).

ECO 1706 Dec '94 change f303 (500 mA) to 1A.

may '95 check AC (R125 stecht).
9500 (FATAL ERROR).

may '95 high ohms (twee weerstanden).

okt '95 option 100 noisy freq.
kristal veranderen.

F/W 4.03 (laatste versie)
F/W 2.06 met 9010 versie 1.
F/W 2.11 (laatste upgrade zonder instinctris)
opt. 250

F/W 3.00 Analog pcb. veranderen (H/W)
Serienummer moet opnieuw worden ingebracht.

MODEL	ITEM
9100	ANALOGUE BOARD

~~LIMITED EFFECT~~ ~~ROUTINE~~

COMPATIBLE / INCOMPATIBLE **CHANGE** **IMMEDIATE**

DATE RELEASED: 12 DEC 1995

ECO 5026 SHT 1 OF 2

PERFORMANCE | MANUFACTURING

REASON FOR CHANGE (ECR No.)

EXISTING COMPONENT HAS HIGH VARIABLE THERMAL COEFF

REDUCES ERRORS 40-399 LO I

DESCRIPTION OF CHANGE

USE BETTER QUALITY COMPONENT.

PROTECTION WILL BE TO ± 200V INSTEAD OF PRESENT 250V BUT THIS IS NOT SPEC'D TO CUSTOMER & FIRMWARE CLAMPS WILL ALSO PROTECT

DOCUMENTATION

DRAWING No.	SHT No.	NEW ISS.REV
DA 401239	2	1.7
LA 401239	ALL	.
DC 401239	3	1.3
LO 401239	ALL	1.14
DA 401239	1	1.4

ACTION	√/X
PROCUREMENT	√
SUB ASSY KITS	√
SUB ASSY ASSEMBLY	√
SUB ASSY TEST	√
INST KITS	√
INST ASSEMBLY	√
INST TEST	√
PRE ALLOCATION STOCK	√
CONFIGURE	√
INST CALIBRATION	√
FINISHED INST STOCK	√
NON MANUFACTURING:	
PRE ALLOCATION STOCK	√
INST TEST	√
INST CALIBRATION	√
FINISHED INST STOCK	√
CUSTOMER SERVICE:	
C/S RETURNS	√
C/S RECALL	NO
UPDATE INSTRUMENT MODIFICATION LEVEL	

REQUESTED/APPROVED		DATE
NAME	C BURN	11/11/95
SECT HD		
ENG MAN		11/12/95
OPS MAN		11/12/95
QA MAN		11 DEC 95
CUST SERV	A. Reddy	11/12/95
MKT MAN		11/12/95

	MECH	ANALOG	DIGITAL	S/W	CHIEF
PRINC ENG					

	PURCH	PR.CTL	ASSY	TEST	M.ENG
PROD MAN					

COMMENT CLEARS STOP SHIP ORDER 92 TOK 95

SS DOES NOT APPLY TO 9000

ASSEMBLY NUMBER	CHANGE FROM (DELETE) DESCRIPTION	PART No.	STK	DES'G OR QTY
DA 401239	34K 2W	007393	U	R356
	39K 2W	007393	U	R354
				A/R
	(NEW PART REQUIRED)			
401239	BEAD CERAMIC 16 SWG	630020	U	4

CHANGE TO (ADD) DESCRIPTION	PART No.	STK
50K 3 ppm 1% 175mW @ 25°C	080185	N
50K 3 ppm 1% 175mW @ 25°C	080185	N
SLEEVING A/R	59000A	
} MAY 50K 000F (ALPHA) - OR		
} S102K 50K 1% (VISHAY)		
RESISTORS <1.0nV/°C MAX 0.1nV/°C TYP		

DATE EFFECTIVE BATCH NUMBERS	
B.No.	
DATE	
B.No.	
DATE	
B.No.	
DATE	
B.No.	
DATE	

EXPECTED COST OF CHANGE	
MATL:	+ £3-00
LABOUR:	
OBS MATL:	
REWORK:	
CAPITAL:	

ECO 5026

WAVETEK LTD. NORWICH ENGLAND

STOCK CODES: U (USED ELSEWHERE) O (OBSOLETE) N (NEW)

RECAL PROCEDURE AFTER FITTING NEW COMPONENTS

(1) IF INSTRUMENT IS TO BE (RE)CALIBRATED :—

1.1 TURN ON 9100 GIVE 2 MINS TO STABILISE

1.2 SELECT Ω (DEFAULT IS ON FOR THIS)

1.3 USE 4W LEAD (I+ TO HI + I- TO LO AT DVM END) INTO 1281 SET TO DCV IN FILTER ON 7½ D

1.4 ADJUST R308 UNTIL DVM READS 0.000V ± 0.000,002V

ie ± 2μV

1.5 CAL MACHINE AS NORMAL

(2) IF INSTRUMENT IS TO BE LEFT 'AS IS' ie IT IS NOT WISHED TO RECALIBRATE

2.1 DO 1.1 – 1.3 ABOVE BUT GIVE 20 MINS WARM UP

IF DVM READS <10μV IT CAN PROCEED WITHOUT RECAL. GO TO 2.3

2.2 RECAL THE MACHINE AS NORMAL IF 2.1 HAS FAILED

2.3 SELECT 45Ω LO I 4W ON 9100, O/P ON
SELECT 7½D 10KΩ 4W RANGE ON 1281 (WHICH MUST HAVE BEEN ZEROED & BE IN CAL)
ADJUST R308 UNTIL 1281 READS 45.000Ω ± 0.003Ω

2.4. PUT 9100 ON CAL SYSTEM & VERIFY OHMS FUNCTION IS IN SPEC (<60ppm) IF THERE ARE ANY FAILS, RECAL.

9100 Analogue Assembly Tests

Equipment

1. 9100 Analogue assy Test rig TR261 (or TR269 if two must be in use at once)
2. 1281 DMM with leads terminated in test hooks
3. DM97 Handheld DMM with adapter lead, dual 4mm to pins spaced 8-12mm
4. Frequency counter Dana 8130
5. Oscilloscope 100 MHz, with 10:1 probe
6. Probe, 10MΩ input impedance, 10:1attenuation
7. Pomona plug with test points inserted
8. Pair of 4mm to 4mm test leads
9. AVO 8 Analogue Multimeter or similar (short circuit I on lowest x1 Ω range must be >60mA)
10. 13V 1A floating Power Supply with adjustable current limit
11. Test link and switches TE 1561
12. Resistance box with 100MΩ max
13. Test piece TE1340 (100kohm in parallel with 100pF)
14. Single lead, 1.5m long, 4mm banana to pointed probe tip
15. Signal Generator

Abbreviations used

w.r.t = with respect to
ESD = Electrostatic Discharge
I.C.T = In Circuit Test
o/p = output
UUT = Unit under Test

Notes

1.0 All faults found and their fixes should be listed on the I.C.T Test Record Sheet.
2.0 Observe ESD precautions throughout these tests.
3.0 "Left" and "right" are looking at the board under test from the front of the instrument.
4.0 Ticksheet to be completed as test progresses.
5.0 All scope settings are final settings. If a scope does not automatically compensate for the 10:1 probe it is necessary to divide the V/div settings given by 10.

1.0 Reference Set up.

1.1 Set the 1281 to DCV, 10V, 6 digits.
Check links TL101-TL105 are intact. If not, go to 1.2 or remake them.
Connect the DMM Lo to TP410 and the Hi to the left side of TL105.
Check the voltage is between +6.792V and +7.066V. If just outside these limits, seek assistance.
Refer to table below and cut links TL101 - TL105 as required.

Voltage	Range	TL105	TL104	TL103	TL102	TL101
7.042	7.066	CUT	-	CUT	-	-
7.017	7.041	CUT	-	-	CUT	CUT
6.992	7.016	CUT	-	-	CUT	-
6.967	6.991	CUT	-	-	-	CUT
6.942	6.966	CUT	-	-	-	-
6.917	6.941	-	CUT	CUT	CUT	CUT
6.892	6.916	-	CUT	CUT	CUT	-
6.867	6.891	-	CUT	CUT	-	CUT
6.842	6.866	-	CUT	CUT	-	-
6.817	6.841	-	CUT	-	CUT	CUT
6.792	6.816	-	CUT	-	CUT	-

1.2 Check the DMM reads between +6.5372V and +6.5699V.

2.0 Derived Supplies check.

2.1 Move DMM Hi to D103 Cathode, check voltage is between +11.5V & +12.6V.
2.2 Clip DMM Hi to D104 Anode, check voltage is between -6.8V & -8.1V.
2.3 Ensure difference 2.1-2.2 is between 18.5V and 20.5V. (This can be read directly by touching DMM Lo to D103 Cathode. Return DMM Lo to TP410).

2.4 Move DMM Hi to Q507em. Check voltage is between +11.5V & +13.3V.
2.5 Clip DMM Hi to Q508em. Check voltage is between -6.5V & -7.5V.
2.6 Ensure difference 2.4-2.5 is between 18.3V and 20.3V. (This can be read directly by touching DMM Lo to Q507em. Return DMM Lo to TP410).

2.7 On the 9100 select Ohms, 1KΩ, o/p ON.

Check w.r.t TP410:-

D601cathode	+4.1V	to +5.5V
D602anode	-4.1V	to -5.5V

(If either fails, check V rating of D601, D602. Zener current should be 4-9mA)

D801anode	-2.0V	to +2.0V
Q614 gate	-6.7V	to -7.3V

Q614's gate is the right hand leg viewed from the front.
Note: Ignore any warning messages on the display.

3.0 AC voltage levels

3.1 Set 1281 to ACV, 10V range, and connect between the Hi & Lo terminals of the UUT, using items 7 and 8. Connect the scope Ch1 set to 0.5V/div, 0.2msec/div across pomona plug item 7, taking care that the scope earth connection goes to the inside Lo terminal of the UUT.
On the 9100 select ACV, 3V, 1KHz, o/p ON. Trigger the scope from Int, Ch1, DC, +ve, Auto.
Check that the DMM indicates between 2.94V and 3.06V.
On the scope, check for no distortion, clipping or oscillation.
On the 1281 select Maths, Config, Z, Last Rdg, Enter, Maths, ÷Z, %.
The 1281 should now read 100.0%.
Select ÷10 on the 9100.
Check for no oscillation on scope, check 1281 reads 9.8 to 10.2%.

3.2 Press x10 on the 9100. On the 9100 select 10KHz.
Check that the 1281 reading is now between 99.9% and 100.1%.
On the 9100 select 100KHz.
Check that the 1281 reading is now between 98.0% and 102.0%.
Cancel –Z & % keys on the 1281.

3.3 On the 1281 select DCV, 100V, Filter ON. Connect the DMM Hi to TP102 and the Lo to TP106.
On the 9100 select ACV, 20V, 55Hz, Sine, o/p ON.
Check the 1281 reads 0v +/- 0.003V.
If not, replace R151 with item 12 set to 320KΩ and adjust the resistance box until the reading is in spec. Replace R151 with the value indicated by the box, if necessary using two resistors to get within 1KΩ. If the value indicated is outside the limits 220KΩ to 560KΩ seek fault finding assistance.

3.4 If R151 has been replaced, allow to cool and repeat section 3.3, noting that the 1281 measurement limit is increased to 0V +/- 0.005V. Remove the 1281 and its test leads.

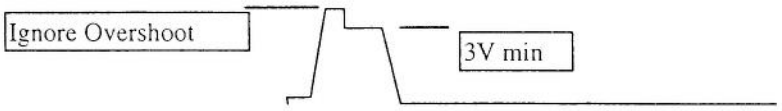
3.5 Connect frequency counter item 4 to 9100 o/p via pomona plug item 7 and probe item 6. Select ACV 5V 900Hz. Connect sig generator item 15 set to TTL 900Hz to the 9100 rear input. Select ΔΦ on the lower then top side soft keys. Turn the 9100 ON.
Ensure the counter is triggering correctly. Vary the sig gen between 900 and 910Hz.
Check the frequency counter tracks. Beware of mistriggering!
Repeat this test, setting the 9100 to 30Hz, and item 15 to 0.3V AC, 30 Hz. Vary it 30-32Hz. and check that the counter tracks with no hint of noise or mistriggering. Remove the frequency counter.

4.0 Frequency

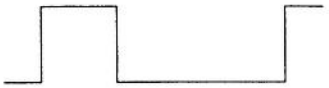
4.1. On the 9100 select Hz, o/p ON, and check that the following frequencies are within the limits shown:-

10Hz	10.00000Hz	±25 digits	(0.00025Hz)
1KHz	1000.000Hz	±25 digit	(0.025Hz)
200KHz	200.000KHz	±5 digits	(5Hz)
201KHz	201.000KHz	±5 digits	(5Hz)
10MHz	10.00000MHz	±25 digits	(250Hz)

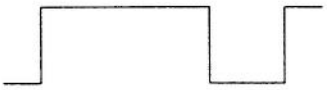
4.2.1 Select Hz, Pulse Width, set pulse width to 0.3µS,(00.0003mS), period to 100 µS. Set scope to display 1V/div, 1µsec/div. Check that the output is 0.3µS positive pulse width.
The pulse amplitude must reach at least 3V after aberrations have died away.



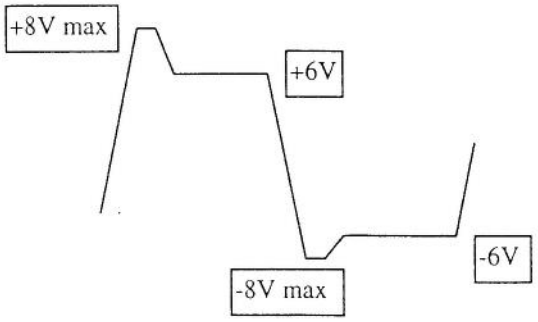
4.2.2 Set period to 15msec, pulse width to 5msec. Set scope to 2msec/div.
Check that the output is 5msec pulse width with a period of 15msec, amplitude 4.75 to 5.25V



4.2.3 Ensure the 9100 cursor is on the pulse width field. Press the INVERT soft key
Check that the signal inverts, i.e the positive section of the waveform now occupies 10msec with the period remaining at 15msec.



4.3 Select Hz, 10MHz, upper voltage limit to +6V, lower voltage limit to -6V. Connect the Test Piece TE1340, item 13, into the pomona plug item 7 already in the 9100. Set the scope to 2V/div, 50nsec/div.
Check that the waveform is roughly sinusoidial, with a peak between +3V and +6.5V and a trough between -3V and -6.5V.
Select 1MHz on the UUT. Set scope to 5V/div, 0.2µsec/div.
Check the waveform is a +/- 6V (+/-0.5V) squarewave with an overshoot peak less than +8.0V and an undershoot peak of less than -8.0V. The risetime should be approx 50nsec, and the waveform settled to 0.1V approx 200nsec after the transition starts.



4.4 Turn the 9100 OFF and remove all test equipment from the UUT.

5.0 Resistance

5.1 Ensure the 9100 is OFF. Fit test link item 11. The box fits to the 1281 Hi, Lo, I+, I-, with the cables exiting to the left. Connect the two trailing pomona plugs to the 9100, red to the Hi /Lo terminals and black to the sHi /sLo terminals, with the ground tags towards the inside of the UUT.
Set every switch to the CLOSED position.
Set the 1281 to100mV, Filter ON, 6 digit, slow.
Press the Zero button on the 1281 and wait until the Busy legend goes out.
Set the SHORT switch to the OPEN position.
On the 9100 select Ohms, 1KΩ, LoI, 4Wire, output ON. (LoI is the lowest setting).
Ignore the warning on the 9100 screen. Adjust R308 until the 1281 reads Zero ± 3.0μV.
Turn 9100 o/p OFF.

5.2 Set 1281 to 1K, 6 digit, filter, 4W.(Do not use Lo current setting).
Set the HIGH switch of the test lead to OPEN, and the SHORT switch to CLOSED.
Press Zero on the 1281. Wait until the Busy light goes out.
Set the HIGH switch of the test lead to CLOSED, the SHORT switch to OPEN and check the 560Ω switch is still at CLOSED.
On the 9100 select zero, LoI, 4W, output ON.
Check the 1281 reads 0+/-0.000010KΩ.
(If this fails, try clearing the cal stores of the 9100. and recheck from 5.1).

5.3 Check CMRR is >10000:1.
On the 1281 enter Maths, Config, C, Last rdg, Enter, Maths, -C. (This sets the 1281 display to zero).
Set the 560Ω switch to OPEN.
(Note:- Under these conditions there should be 0.56V between the 1281 I+ and 9100 Hi).
Note 1281 reading; if it is between +/-0.000045proceed to section 5.5.

5.4 Fit Resistance box item 12 in place of R334. Adjust box so that 1281 reads 0+/- 0.000010KΩ.
Replace box with resistor(s) of total value as indicated by the box +/-100KΩ.
(4.7M to 100M may be required, if outside these limits, check R342, if OK change R314 and start section 5 again).
After allowing at least 2 minutes to cool and for thermals to equalise, check 1281 reads 0+/-0.000020KΩ.

5.5 Cancel -C on 1281. Set the 560Ω switch to CLOSED.
Note 1281 reading A.
Reverse both plugs at the 9100 end, i.e swop Hi and Lo, then sHi and and sLo so that the ground tags both face outwards.
Note 1281 reading B.
If both A and B are 0+/-0.000010KΩ no action is required.
If necessary, readjust R308 and repeat 5.5 until both A and B read less than 0+/-0.000010KΩ and their errors from zero are of equal magnitude.
Remove the test link TE1561 and the 1281.

5.6 On the AVO 8 select the X1ohm range, short circuit the input leads item 8 and adjust to zero.
Connect the AVO 8 to the Hi and Lo terminals of the 9100. On the 9100 select Ohms, Zero, Super Current, 2W, o/p ON.
Check the AVO can be adjusted to zero.
Set the 9100 to 20 ohms and check the AVO indicates 18Ω to 22Ω.
Reset the 9100 to zero
Reverse the connections on the AVO, and check it can still be adjusted to zero.
Set the 9100 to 20 ohms and check the AVO indicates 18Ω to 22Ω.
Remove the AVO.

5.7 Check clamps operation.
On the 9100 select Ohm, 10KΩ, 2W, Output ON.
Set the 13V floating power supply item 10 to current limit at 600mA. Turn OFF.
Connect power supply -ve to 9100 Hi using one lead from item 8.
Connect the banana plug of lead item 13 into power supply +ve. Turn Power Supply ON
Momentarily touch the probe tip of lead item 13 to 9100 Chassis. and check the 9100 o/p immediately turns OFF.
Swop the banana plug from the 9100 Hi to the Lo.
Turn the 9100 O/P back ON. Momentarily touch the probe to 9100 Chassis and check the 9100 o/p immediately turns OFF. Swop the leads at the power supply end.
Turn the 9100 O/P back ON. Momentarily touch the probe to 9100 Chassis and check the 9100 o/p immediately turns OFF. Turn the 9100 O/P back ON.
Swop the banana from the 9100 Lo to the Hi.
Turn the 9100 O/P back ON. Momentarily touch the probe to 9100 Chassis and check the 9100 o/p immediately turns OFF.

5.8 Turn the power supply OFF and disconnect the test leads.

6.0 Capacitance

6.1 Ensure nothing is connected to the DM97 item 3. Turn on the DM97, by selecting Cap on the rotary dial. When it displays 0.000nF connect the DM97 to the UUT Hi/Lo terminal pair and sHi/sLO sense terminal pair using the adapter lead provided. Do not use the I+/I- pair!
On the 9100 select AUX, Cap, 4W, 2.0nF, o/p ON. (If necessary wait for a self cal to complete.)

6.2 Set the 9100 and DM97 as shown and check that the displayed reading is correct:-

9100	**DM97 range**	**reading**
2nF	4nF	1.88nF to 2.28nF
20nF	40nF	18.1nF to 22.1nF
205nF	400nF	185nF to 225nF. Note reading.

Reverse leads, check for same reading +/- 3 digits. Fail indicates Q617 leaky. Replace Leads.
Increase 9100 output to 205.2nF, while listening for K302 to operate.
Verify handheld reading has increased by between 0.1nF and 0.3F.

2uF	4uF	1800nF to 2200nF
20uF	40uF	18uF to 22uF
200uF	400uF	180uF to 220uF
2mF	4mF	1800uF to 2200uF
20mF	40mF	18mF to 22mF

6.3 Remove the test leads and turn the DMM OFF.

7. Chopper Amp Span

7.1 On the UUT select DCV 0V o/p ON. Check that the following points are within the range +/-3.5V wrt TP410 or chassis, as convenient.

CHECK POINT	Controlled IC
U110/6	U111
U607/6	U602
U608/6	U605
U905/6	U904

(If any point fails, replace the controlled IC noted above. If this fixes the problem, return the removed part to QA. It is failing its offset spec, and the manufacturer must be informed.
Alternatively, there is always a chain of three resistors in series with the pin 6 which was checked. Verify the values in the chain are correct.)

8. Self Test

Note:-The top cover should be laid in place during Self Test as some measurements are light-sensitive.

8.1 Select Mode, Test, 741258 (the password), Enter, and then press the upper vertical soft key to enable factory limits.

A small *f* should appear in the lower right hand corner of the display to indicate that the factory limits are selected. Press FULL.

Ensure that Self Test runs to completion with no failures.

9.0 On completion

9.1 Trim any links cut in test 1.01close to the pcb.
9.2 Sign and date a tested label and fix to the UUT.
9.3 Sign and date the completed Tick List.
9.4 Remove all test equipment from the UUT.

9100 Analogue Assembly Tests

Ticklist

1.0 Reference set up..... ( )
2.0 Derived supplies check..... ( )
3.0 AC Voltage levels..... ( )
4.0 Frequency..... ( )
5.0 Resistance..... ( )
6.0 Capacitance..... ( )
7.0 Chopper spans..... ( )
8.0 SelfTest..... ( )
9.0 On completion..... ( )

Failure Test Reference	Fault Found	Fix	Fixed by:-

Serial No._____ Date _____ Initials_____

Notes:

9000 Power Board Test Procedure

Equipment

1. Oscilloscope with x10 and x100 probes.
2. 1081 or 1281 DMM.
3. Handheld DMM
4. Inductive load TE1268
5. 190pF load TE1278
6. Copper short (Pomona plug type)

Abbreviations used

I.C.T = In Circuit Test
ESD = ElectroStatic Discharge
BUT = Board Under Test
DMM = Digital MultiMeter
wrt = with respect to

Notes

1. All faults found and their fixes should be listed on the I.C.T Test Record Sheet.

2. Observe ESD precautions throughout this procedure.

3. The ±7.5V supplies used by the Current function on this Assy have the capability to deliver > ±20A. If a fault exists this level of current could cause serious damage to the Assy. The In Circuit Tester (ATE) should have found any such fault before the Assy reaches the board level test stage but as a further precaution the ±7.5V supplies are not connected until they are required.
   During the Voltage Function checks the 7 hex studs fixing the BUT to the ±7.5V supplies and blue caps are left out and a suitable insulator fitted between E501,E502,E503 and the ±7.5V secondaries of the test rig.

Preliminary

1. Remove F501, F502, F503, F504.

2. Check R415, 420, 422, 424, 443, 435, 437, 439 are all vertical and have a gap of at least 2 mm from their nearest components.

3. Fit a copper short between the I+ and I- terminals of the test rig.

Procedure

VOLTAGE CHECKS

1.0 Connect BUT to test rig. DO NOT connect the high current secondaries. Ensure J501, J701 and J801 one PSU and two ribbon cables are connected.
Ensure star points and LF TX lugs are screwed down.

** FIT INSULATOR BEHIND HIGH CURRENT BUS BARS **

2.0 Switch on and check for overheating components, especially: R411, R403, Q409, Q407, Q309, Q306, R415, R420, R422, R424, R439, R437, R435, R443.

Note: The display will be blank at this stage.

3.0 Using 1081 DMM, check the following voltages wrt TP112:-

TP515	+ 5.5V	± 0.25V
TP514	+11.8V	± 0.50V
TP512	+15.0V	± 0.25V
TP513	-15.0V	± 0.25V

Switch off power.

4.0 Fit F503 and F504. (±70V fuses).
Ensure that R208 bias adjust pot is set fully counterclockwise.
Switch on power and check the following voltages wrt TP112 using 1081:-

TP213	+70V	± 7V
TP223	-70V	± 7V
TP520	-22V	± 1.5V
TP102	0V	± 10mV

Note: The display should now be fully operational.

5.0 Connect Handheld DMM to TP213 wrt TP214.
Select ACV,3.3V 1KHz,Output ON.
Adjust R208 until the Handheld DMM indicates +300mV ± 10 mV.
The reading will increase slowly then fall back and then increase rapidly.
(Do this carefully as it is possible to exceed 500mA which would strain the fuses F503, F504.(70V fuses))
Nb. At very low bias levels a low level oscillation will be present.

6.0 While monitoring output with scope and 1081 DMM, exercise the amplifier by demanding:-

+32V)
+3.3V)
-3.3V)
-32V)
32V/1KHz) Check for obvious aberrations
32V/100KHz) or oscillations.

Switch off and fit F501 and F502.(±200V fuses).

DANGEROUS VOLTAGES WILL BE PRESENT FROM THIS POINT.

7.0 Select 3.3V/1KHz, output ON.
Check Handheld DMM reads +300mV ± 10 mV
Note: test rig output must not be loaded.

Select 33V/1KHz, output ON.
Check Handheld DMM reads +300mV ± 40mV
Note: test rig output must not be loaded.

8.0 With scope and 1081 DMM on output, exercise amplifier by demanding:-

105V/1KHz) Check with scope for
105V/100KHz) aberrations/oscillations

9.0 Check overcurrent trip on the ± 200V PSU by decreasing output demand to 33V/1KHz and carefully adjust R208 clockwise while monitoring TP213 wrt TP214 with the Handheld DMM. The trip point should be +1.800V to +2.200V. Do not increase beyond +2.2V as this indicates a fault and damage might occur. Reduce demand to 3.3V/1KHz output ON and back off R208 until Handheld DMM reads +300 mV ± 10 mV.

This completes the basic functional testing of the HVPA core and HVPSU switch. Damage to either of these due to a fault in the outer 300V/1KV loops is unlikely.

10.0 Check the following with a scope and 1081 DMM on output:

+33 V DC)
-33 V DC)
+320 V DC)
-320 V DC) Monitor TP102 wrt TP112
+330 V DC) using the Handheld DMM
-330 V DC) and ensure that it remains

+1050 V DC	)	within ± 25V
-1050 V DC	)	
106 V/40Hz	)	
320 V/40Hz	)	Monitor TP106 wrt TP112
330 V/40Hz	)	using the Handheld DMM and
1050V/40Hz	)	ensure it remains within
106 V/30KHz	)	± 10V
320 V/30KHz	)	
330 V/30KHz	)	
1050V/10KHz	)	

11.0 Full load test.
Connect Hi to sHi and Lo to sLo.Connect the 190pF load TE1278 between Hi and Lo.
Connect the Handheld DMM to TP213 wrt TP214.
Select 350V 30KHz, Output ON.The reading should stabilize to below 1.65V within approx 20 secs.

13.0 Press Mode,MANUAL.

CURRENT CHECKS

Note: For all subsequent tests use the 1081 DMM and x10 scope probe. DMM ground wrt. TP302 and scope grounds are taken to chassis unless advised otherwise.

Switch on and check for overheating components, especially: R411, R403, Q409, Q407, Q309, Q306, R415, R420, R422, R424, R439, R437, R435, R443.

14.0 Open loop bias checks:

Move J803 to the right. Output off.
Check that the following measurements are within the limits shown:-

V-I:	TP304	-11mV to 11mV
DC Servo:	U308 pin 6	-1.1V to +1.1V
	Across R331	25mV to 50mV
	Across R307	25mV to 50mV
lo I output:	Across R402	0.4V to 1V
	Across R410	0.4V to 1V
	Across R403	0.4V to 1V
	Across R411	0.4V to 1V
Local PSU	U308 pin 4	-3.75V to -6.25V
	U308 pin 7	+3.75V to +6.25V
	U301 pin 13	+8.4V to +10.4V

Move J803 to the left.

15.0 3mA and 300 mA range checks:

Connect 1081 and scope to TP310.
Check that the following outputs are within the limits shown:-

Output	TP310
3.2mA 30KHz	1.061V to 1.072V
320mA 30KHz	1.061V to 1.072V

No signs of oscillation or distortion should be visible on scope.

16.0 Select DCI,ZERO,Output ON. Measure TP301 wrtTP302.
Adjust output until 1081 reads 0V ± 10µV.
Measure TP314 wrt TP312.
1081 should read 0V ± 20µV.

17.0 3A range bias check:

Turn rig off then connect ±7V5 caps and power supplies to power board via E501-E507

Connect scope to TP308.

Connect the DMM across R415.
Power up rig and check that the DMM reading is between 79mV and 120mV.
Connect the DMM across R443 and check that the DMM reading is between 79mV and 120mV.
Check for overheating components, especially: R411, R403, Q409, Q407, Q309, Q306, R415, R420, R422, R424, R439, R437, R435, R443.
Turn rig off if either reading is outside range or any componets are overheating and investigate using a bench supply as detailed in Appendix 1.

Ensure that the scope does not show oscillation.

Check that the following voltages are within the limits shown:-

across R420	-1mV to +1mV
across R435	-1mV to +1mV
across D414	1.85V to 2.2V
across D416	1.85V to 2.2V

Calculate and check against limits:-

Voltage across R415-Voltage across R443 = -10mV to +10mV

18.0 3A range

Connect DMM and scope to TP310.
Check that the following outputs are within the limits shown:-

Output	TP310
+3.2A	-105.1mV to -108.0mV
-3.2A	105.1mV to 108.0mV
3.2A 10KHz	104.1mV to 108.0mV

No signs of oscillation or distortion should be visible on the scope.

19.0 30A range bias check:

Select +3.3A.

Connect the scope to TP309.

Connect DMM across R435.
Check for a reading of 0V ± 1mV.
Connect DMM across R420.
Check for a reading of 0V ± 1mV.

Press Output ON and check that the reading increases to 185mV ± 30mV.

Ensure that the scope does not show oscillation.

Return the DMM to across R435 and check that the reading is 95mV ± 26mV.

Calculate and check against limits:-

Voltage across R420-Voltage across R435 = +90mV ± 25mV

With +3.3A,Output ON still selected measure:-

Voltage across R420)	Check that all readings are
)	185mV ± 30mV and that the
Voltage across R422)	highest and lowest readings
)	are within 20mV
Voltage across R424)	
Voltage across R415)	Check that this is greater that the average reading measured above by 20mV to 40mV.

Select -3.3A,Output ON. Measure:-

Voltage across R435)) Voltage across R437)) Voltage across R439)	Check that all readings are 185mV ± 30mV and that the highest and lowest readings are within 20mV
Voltage across R443)	Check that this is greater that the average reading measured above by 20mV to 40mV.

20.0 30A range checks:

Note: Perform test (20) quickly as output is limited to <2 mins @ 20A.

Connect DMM and scope to TP310.
Check that the following outputs are within the limits shown:-

Output	TP310
+20A	-98.6mV to -101.4mV
-20A	+98.6mV to +101.4mV
20A -10KHz	95.7mV to 99.3mV

No signs of oscillation or distortion should be visible on the scope.

21.0 Inductive load tests

Connect the Inductive load TE1268 to the I+ and I- terminals of the test rig. Connect a scope between I+ and the chassis using a x10 probe. Check that the following outputs can be selected without the scope showing oscillation or the overload detector tripping:-

Outputs	Loads
3.2mA 10Hz	30uH
320mA 10Hz	30uH
3.2A 10Hz	18.4uH
10.5A 10Hz	5.5uH

22.0 Selftest

Perform a FULL Selftest against f limits ensuring that there are no failures.

Repeat relevant sections of this procedure if component replacement is required.

23.0 This completes the tests.
Sign and date a tested label and fix to the BUT.

Appendix 1

To investigate faults on the 3A and 20A ranges it is advisable to operate the circuit from a bench supply in order to limit the maximum current available to the BUT,(see note 3 on Sheet 1).

Most In-House supplies are limited to 2A max.

Procedure:-

Remove studs from E501,E502,E503 and fit an insulator between these and the test rig ± 7.5V secondaries.

Connect bench supply as follows:-

+7.5V to E504
0V to E505
-7.5V to E507

IMPORTANT : The following Power up/Power down sequence must be adhered to or damage will occur:-

1.Rig on
2.Bench supply on
3.Bench supply off
4.Rig off

The 3A range can now be investigated by monitoring TP310 with a DMM and scope:-

Output	TP310
+1A	+32.8mV to +33.8mV
-1A	-32.8mV to -33.8mV
1A 10Hz	32.8mV to 33.8mV
1A 10KHz	32.5mV to 33.8mV

9100 Power Board Test Procedure

Equipment

1. Oscilloscope with x10 and x100 probes.
2. 1081 or 1281 DMM.
3. Handheld DMM
4. Inductive load TE1268
5. 190pF load TE1278
6. Copper short (Pomona plug type)
7. 700uH Inductive load

Abbreviations used

I.C.T = In Circuit Test
ESD = ElectroStatic Discharge
BUT = Board Under Test
DMM = Digital MultiMeter
wrt = with respect to

Notes

1. All faults found and their fixes should be listed on the I.C.T Test Record Sheet.

2. Observe ESD precautions throughout this procedure.

3. The ±9.5V supplies used by the Current function on this Assy have the capability to deliver > ±20A. If a fault exists this level of current could cause serious damage to the Assy. The In Circuit Tester (ATE) should have found any such fault before the Assy reaches the board level test stage but as a further precaution the ±9.5V supplies are not connected until they are required.
During the Voltage Function checks the 7 hex studs fixing the BUT to the ±9.5V supplies and blue caps are left out and a suitable insulator fitted between E501,E502,E503 and the ±9.5V secondaries of the test rig.

Preliminary

1. Remove F501, F502, F503, F504.

2. Check R415, 420, 422, 424, 443, 435, 437, 439 are all vertical and have a gap of at least 2 mm from their nearest components.

3. Fit a copper short between the I+ and I- terminals

of the test rig.

Procedure

VOLTAGE CHECKS

1.0 Connect BUT to test rig. DO NOT connect the high current secondaries. Ensure J501, J701 and J801 one PSU and two ribbon cables are connected.
Ensure star points and LF TX lugs are screwed down.

** FIT INSULATOR BEHIND HIGH CURRENT BUS BARS **

2.0 Switch on and check for overheating components, especially: R411, R403, Q409, Q407, Q309, Q306, R415, R420, R422, R424, R439, R43Z, R435, R443.

Note: The display will be blank at this stage.

3.0 Using 1081 DMM, check the following voltages wrt TP112:-

TP515	+ 5.5V	± 0.25V
TP514	+11.8V	± 0.50V
TP512	+15.0V	± 0.25V
TP513	-15.0V	± 0.25V

Switch off power.

4.0 Fit F503 and F504. (±70V fuses).
Do NOT fit F501/F502 yet

Ensure that R208 bias adjust pot is set fully counterclockwise.
Switch on power and check the following voltages wrt TP112 using 1081:-

TP213	+70V	± 7V
TP223	-70V	± 7V
TP520	-22V	± 1.5V
TP102	0V	± 10mV

Note: The display should now be fully operational.

5.0 Connect Handheld DMM to TP213 wrt TP214.
Select ACV, 3.3V 1KHz, Output ON and unloaded.
Adjust R208 until the Handheld DMM indicates +300mV ± 10 mV.
The reading will increase slowly then fall back and then increase rapidly.
(Do this carefully as it is possible to exceed 500mA which would strain the fuses F503, F504.(70V fuses))
Nb. At very low bias levels a low level oscillation will be present.

6.0 While monitoring output with scope and 1081 DMM, exercise the amplifier by demanding:-

+32V)
+3.3V)
-3.3V)
-32V)
32V/1KHz) Check for obvious aberrations
32V/100KHz) or oscillations.

Switch off and fit F501 and F502.(±200V fuses).

DANGEROUS VOLTAGES WILL BE PRESENT FROM THIS POINT.

7.0 Select 3.3V/1KHz, output ON.
Check Handheld DMM reads +300mV ± 10 mV
Note: test rig output must not be loaded.

Select 33V/1KHz, output ON.
Check Handheld DMM reads +300 mV ± 40mV
Note: test rig output must not be loaded.

8.0 With scope and 1081 DMM on output, exercise amplifier by demanding:-

105V/1KHz) Check with scope for
105V/100KHz) aberrations/oscillations

9.0 Check overcurrent trip on the ± 200V PSU by decreasing output demand to 33V/1KHz and carefully adjust R208 clockwise while monitoring TP213 wrt TP214 with the Handheld DMM. The trip point should be +1.800V to +2.200V. Do not increase beyond +2.2V as this indicates a fault and damage might occur. Reduce demand to 3.3V/1KHz output ON and back off R208 until Handheld DMM reads +300 mV ± 10 mV.

This completes the basic functional testing of the HVPA core and HVPSU switch. Damage to either of these due to a fault in the outer 300V/1KV loops is unlikely.

10.0 Check the following with a scope and 1081 DMM on output:

+33 V DC)
-33 V DC)

+320 V DC	)
-320 V DC	) Monitor TP102 wrt TP112
+330 V DC	) using the Handheld DMM
-330 V DC	) and ensure that it remains
+1050 V DC	) within ± 25V
-1050 V DC	)

106 V/40Hz	)
320 V/40Hz	) Monitor TP106 wrt TP112
330 V/40Hz	) using the Handheld DMM and
1050V/40Hz	) ensure it remains within
106 V/30KHz	) ± 10V
320 V/30KHz	)
330 V/30KHz	)
1050V/10KHz	)

11.0 Full load test.
Connect Hi to sHi and Lo to sLo. Connect the 190pF load TE1278 between Hi and Lo.
Connect the Handheld DMM to TP213 wrt TP214.
Select 350V 30KHz, Output ON. The reading should stabilize to below 1.65V within approx 20 secs.

13.0 Press Mode,MANUAL.

CURRENT CHECKS

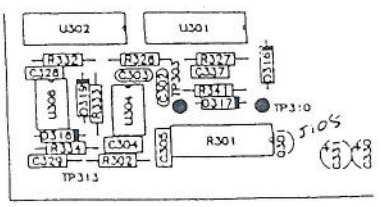
Note: For all subsequent tests use the 1081 DMM and x10 scope probe. DMM ground wrt. TP302 and scope grounds are taken to chassis unless advised otherwise.

Switch on and check for overheating components, especially: R411, R403, Q409, Q407, Q309, Q306, R415, R420, R422, R424, R439, R437, R435, R443.

14.0 Open loop bias checks:

Move J803 to the right. Output off.
Check that the following measurements are within the limits shown:-

V-I:	TP304	-11mV to 11mV
Local PSU	U308 pin 4	-3.75V to -6.25V
	U308 pin 7	+3.75V to +6.25V
	U301 pin 13	+8.4V to +10.4V
DC Servo:	U308 pin 6	-1.1V to +1.1V
	Across R331	25mV to 50mV
	Across R307	25mV to 50mV
lo I output:	Across R402	0.4V to 1V
	Across R410	0.4V to 1V
	Across R403	0.4V to 1V
	Across R411	0.4V to 1V



Move J803 to the left.

15.0 3mA and 300 mA range checks:

Connect 1081 and scope to TP310.
Check that the following outputs are within the limits shown:-

Output	TP310
3.2mA 30KHz	1.061V to 1.072V
320mA 30KHz	1.061V to 1.072V

No signs of oscillation or distortion should be visible on scope.

16.0 Select DCI, ZERO, Output ON. Measure TP301 wrt TP302.
Adjust output until 1081 reads 0V ± 10µV.
Measure TP314 wrt TP312.
1081 should read 0V ± 20µV.

17.0 3A range bias check:

Turn rig off then connect ±7V5 caps and power supplies to power board via E501-E507

Connect scope to TP308.

Connect the DMM across R415. Connect another DMM across R443. Power up rig and check that the DMM's reading are between 79mV and 120mV.
Check for overheating components, especially: R411, R403, Q409, Q407, Q309, Q306, R415, R420, R422, R424, R439, R437, R435, R443.
Turn rig off if either reading is outside range or any components are overheating and investigate using a bench supply as detailed in Appendix 1.

Ensure that the scope does not show oscillation.

Check that the following voltages are within the limits shown:-

across R420	-1mV to +1mV
across R435	-1mV to +1mV

Calculate and check against limits:-

Voltage across R415-Voltage across R443 = -10mV to +10mV

18.0 3A range

Connect DMM and scope to TP310.
Check that the following outputs are within the limits shown:-

Output	TP310
+3.2A	-105.1mV to -108.0mV
-3.2A	105.1mV to 108.0mV
3.2A 10KHz	104.1mV to 108.0mV

No signs of oscillation or distortion should be visible on the scope.

19.0 30A range bias check:

Select +3.3A.

Connect the scope to TP309.

Connect DMM across R420. Connect another DMM across R435.
Check for readings of 0V ± 1mV.

Repeated. sec. 17.

Press Output ON and check that the readings increase to 185mV ± 30mV across R420 and 95mV ± 26mV across R435.

Ensure that the scope does not show oscillation.

Calculate and check against limits:-

Voltage across R420-Voltage across R435 = +90mV ± 25mV

With +3.3A, Output ON still selected measure:-

Voltage across R420)	Check that all readings are
)	185mV ± 30mV and that the
Voltage across R422)	highest and lowest readings
)	are within 20mV
Voltage across R424)	
Voltage across R415)	Check that this is greater than the average reading measured above by 20mV to 40mV.

Select -3.3A, Output ON. Measure:-

Voltage across R435)	Check that all readings are

Voltage across R437) Voltage across R439)	185mV ± 30mV and that the highest and lowest readings are within 20mV
Voltage across R443)	Check that this is greater than the average reading measured above by 20mV to 40mV.

20.0 30A range checks:

Note: Perform test (20) quickly as output is limited to <2 mins @ 20A.

Connect DMM and scope to TP310.
Check that the following outputs are within the limits shown:-

Output	TP310
+20A	-98.6mV to -101.4mV
-20A	+98.6mV to +101.4mV
20A -10KHz	95.7mV to 99.3mV

No signs of oscillation or distortion should be visible on the scope.

21.0 Inductive load tests

Connect the Inductive load TE1268 to the I+ and I- terminals of the test rig. Connect a scope between I+ and the chassis using a x10 probe. Check that the following outputs can be selected without the scope showing oscillation or the overload detector tripping:-

Outputs	Loads
3.2mA 10Hz	30uH
320mA 10Hz	30uH
3.2A 10Hz	18.4uH
10.5A 10Hz	5.5uH

150A 10Hz 700uH (10 turn coil)
increase output slowly to 200A check for no oscillation or the overload detector tripping

22.0 Selftest

Perform a FULL Selftest against *f* limits ensuring that there are no failures.

Repeat relevant sections of this procedure if component replacement is required.

23.0 This completes the tests.
Sign and date a tested label and fix to the BUT.

Appendix 1

To investigate faults on the 3A and 20A ranges it is advisable to operate the circuit from a bench supply in order to limit the maximum current available to the BUT, (see note 3 on Sheet 1).

Most In-House supplies are limited to 2A max.

Procedure:-

Remove studs from E501,E502,E503 and fit an insulator between these and the test rig ± 9.5V secondaries.

Connect bench supply as follows:-

+9.5V to E504
0V to E505
-9.5V to E507

IMPORTANT : The following Power up/Power down sequence must be adhered to or damage will occur:-

1.Rig on
2.Bench supply on
3.Bench supply off
4.Rig off

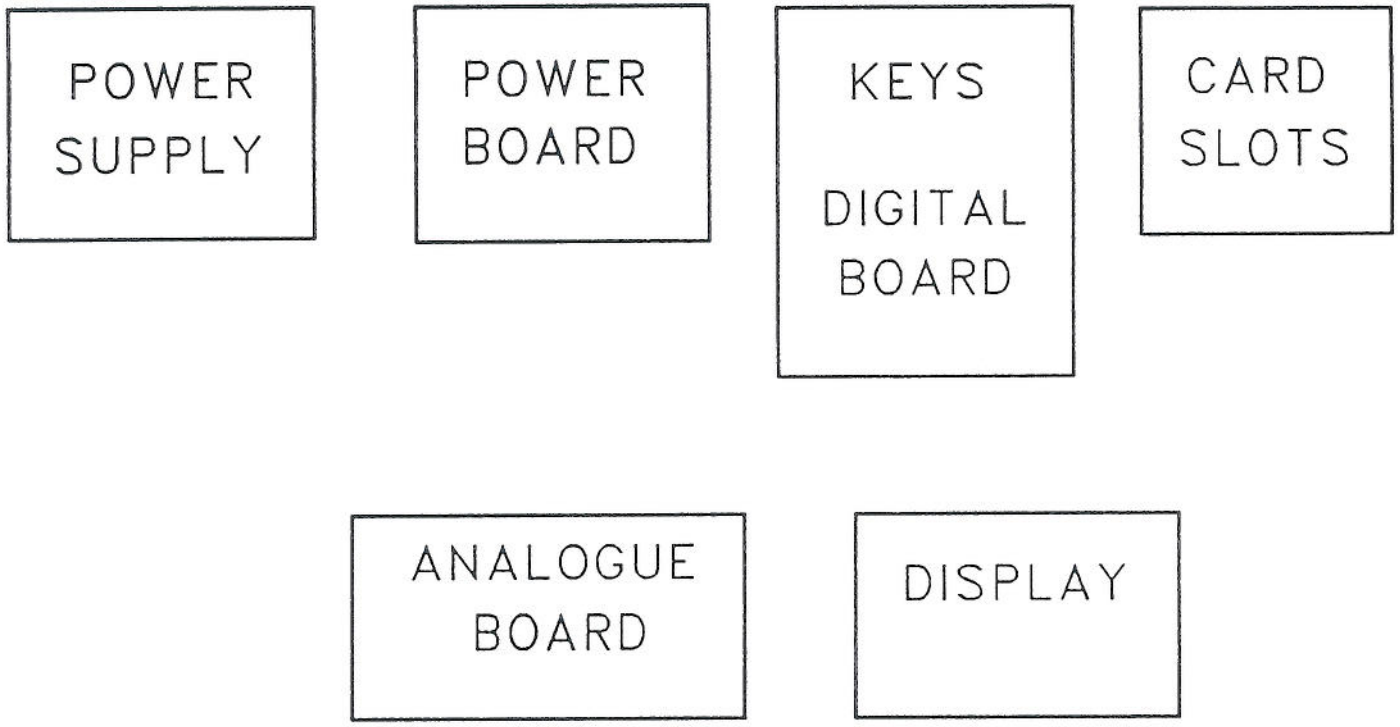
The 3A range can now be investigated by monitoring TP310 with a DMM and scope:-

Output	TP310
+1A	+32.8mV to +33.8mV
-1A	-32.8mV to -33.8mV
1A 10Hz	32.8mV to 33.8mV
1A 10KHz	32.5mV to 33.8mV

Instrument Architecture

Functional Overview

Self Test Overview



9000 MODULES

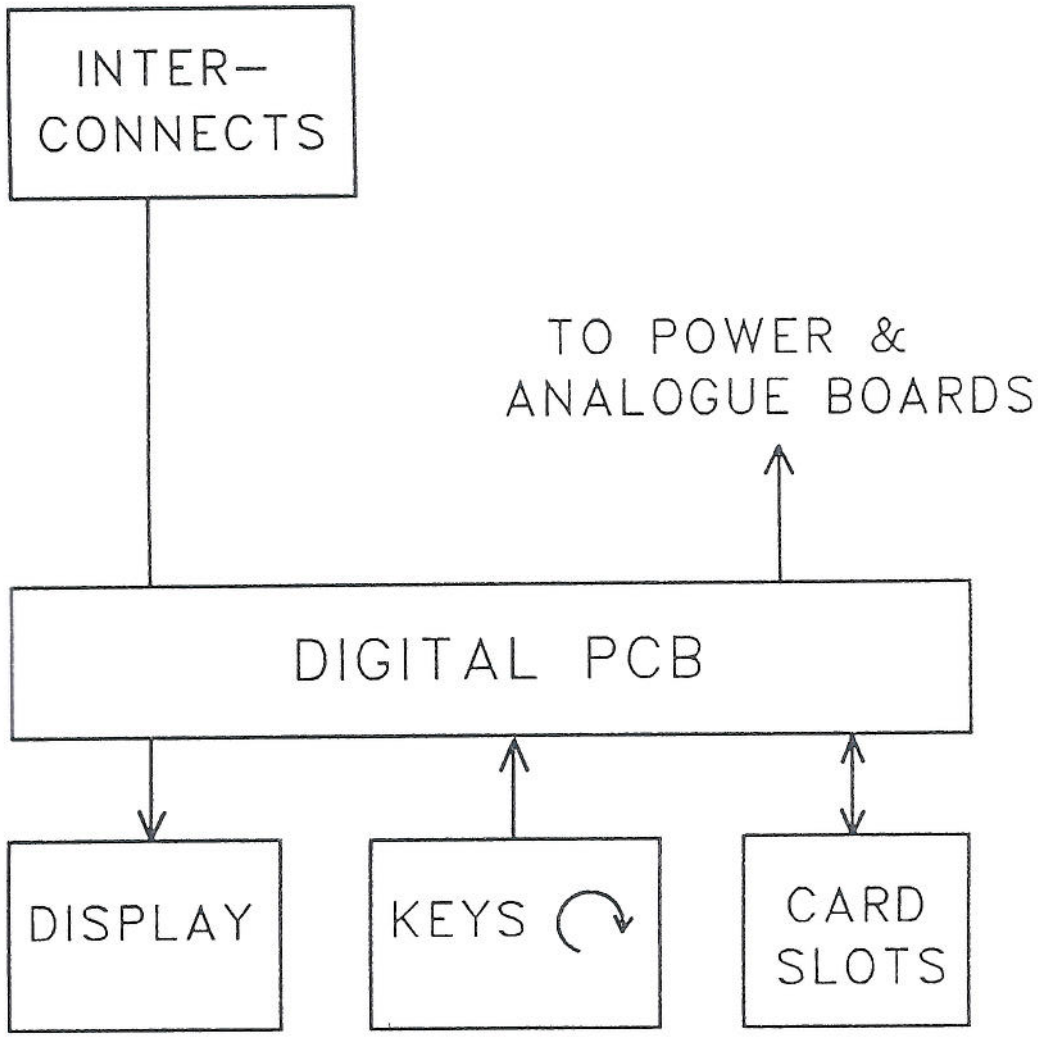
IA1

C38

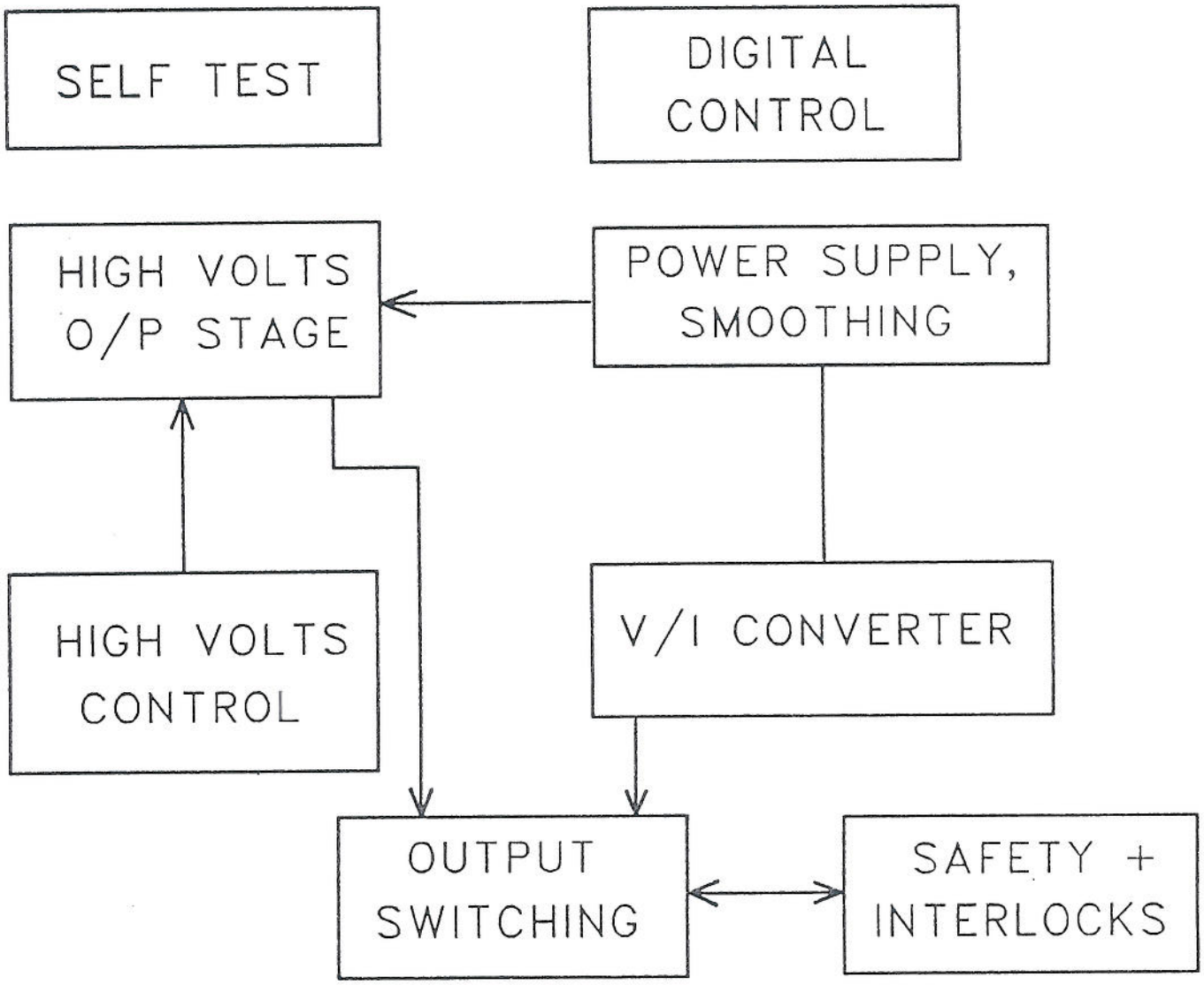
LINEAR POWER SUPPLY

HEAVY
"QUIET" (RFI)
CHEAP?
SIMPLE TO FIX!
200V or
20A
NO LOCAL SWITCHERS
(EXCEPT DISPLAY)

IA2



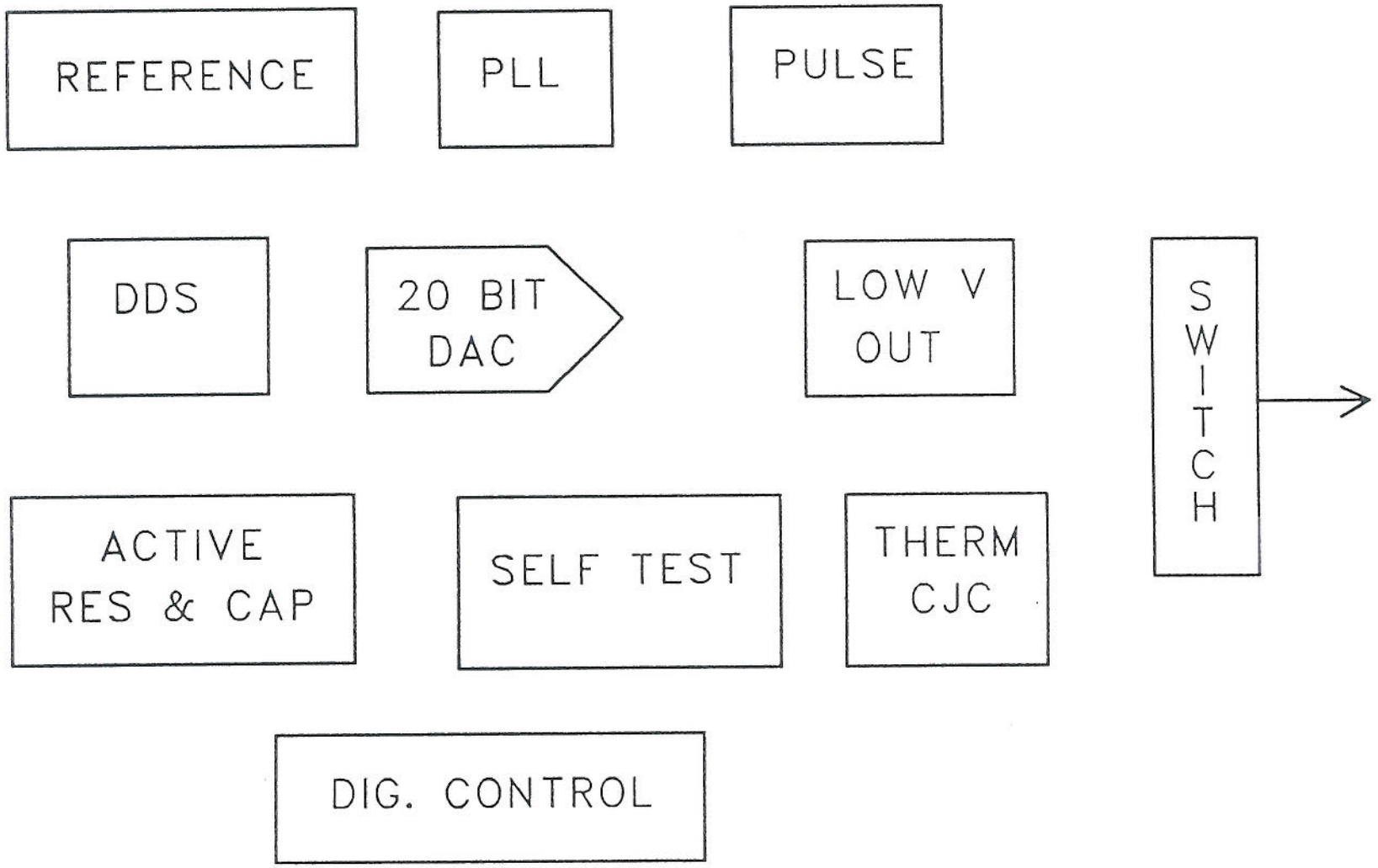
DIGITAL MODULES IA3



POWER BOARD MODULES

IA4

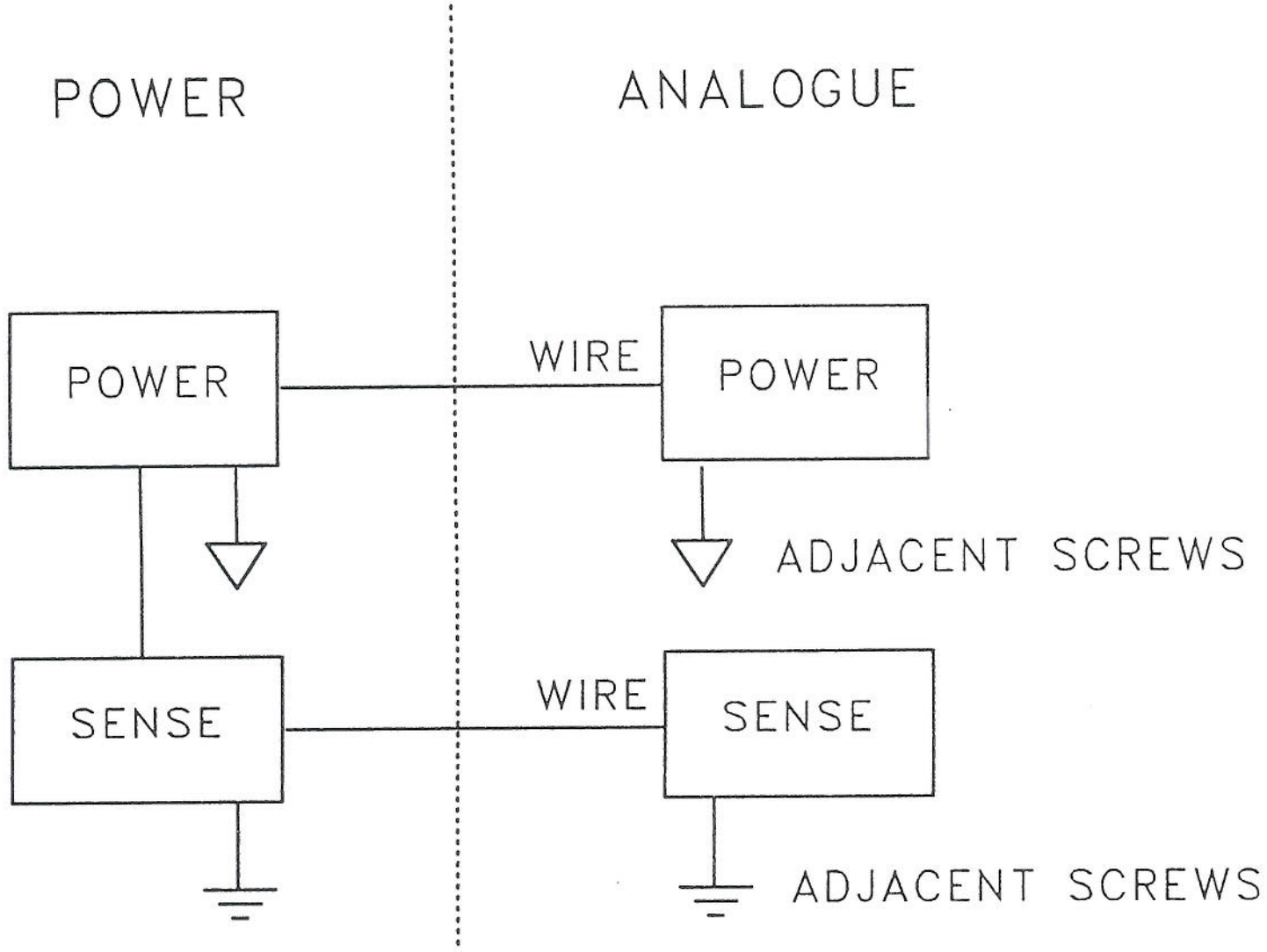
C41



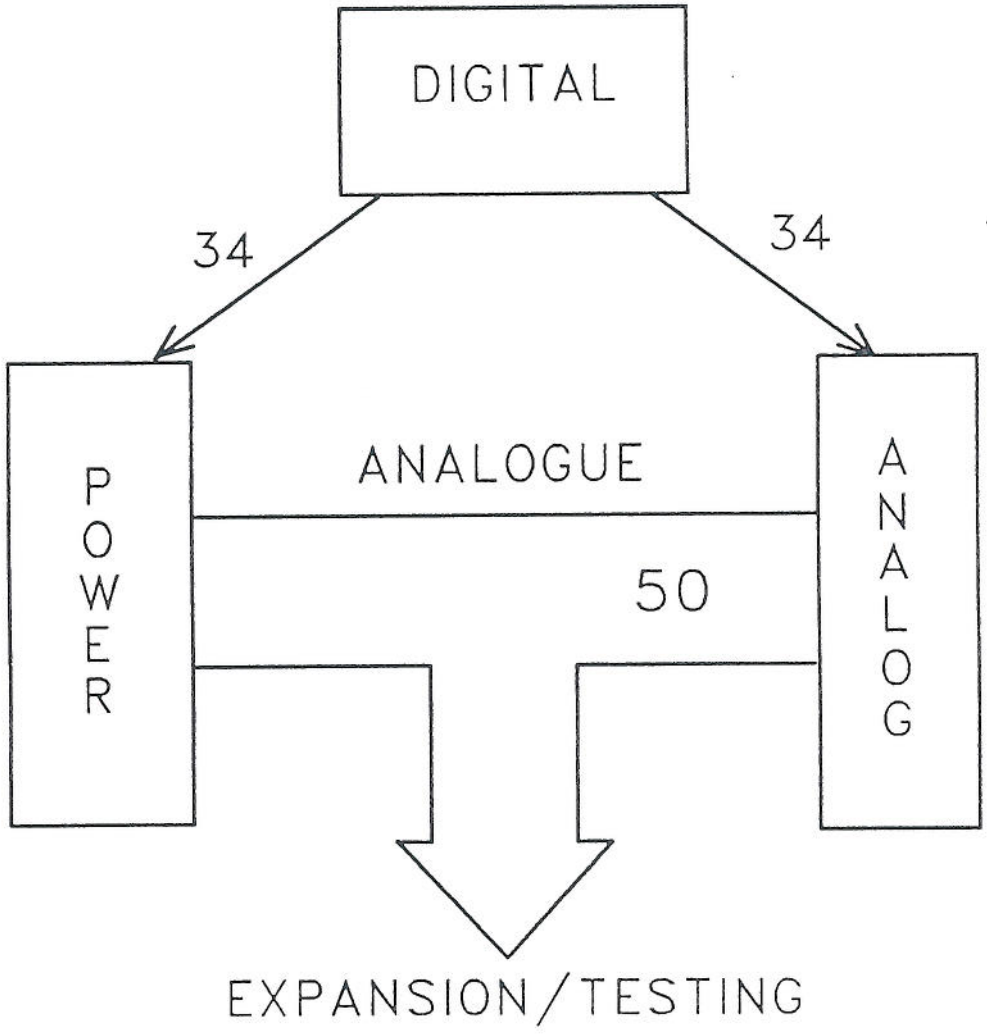
ANALOGUE BOARD MODULES

IA5

C42

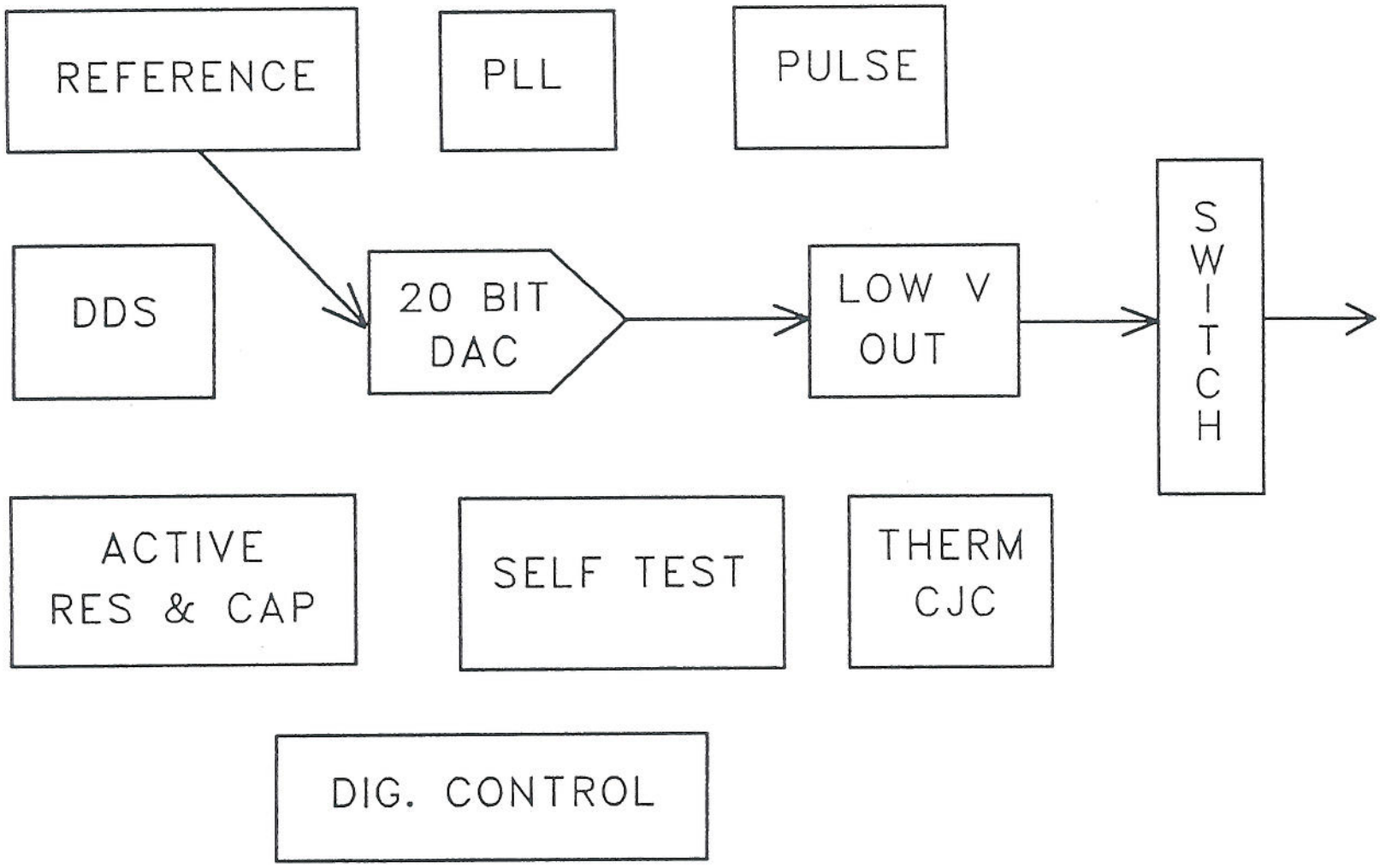


POWER STARS IA6



BOARD INTERCONNECTS

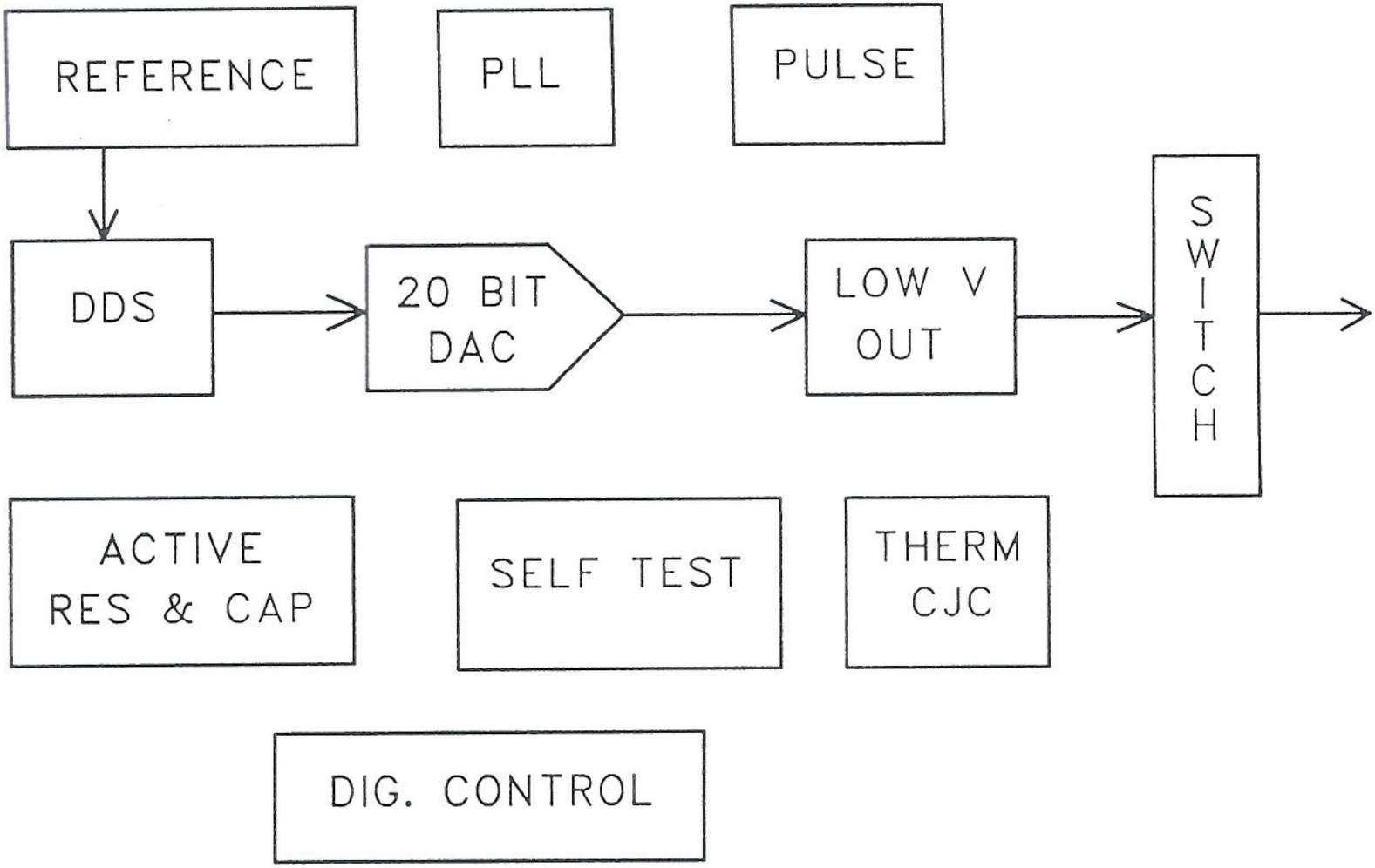
IA7



LOW VOLTS DC

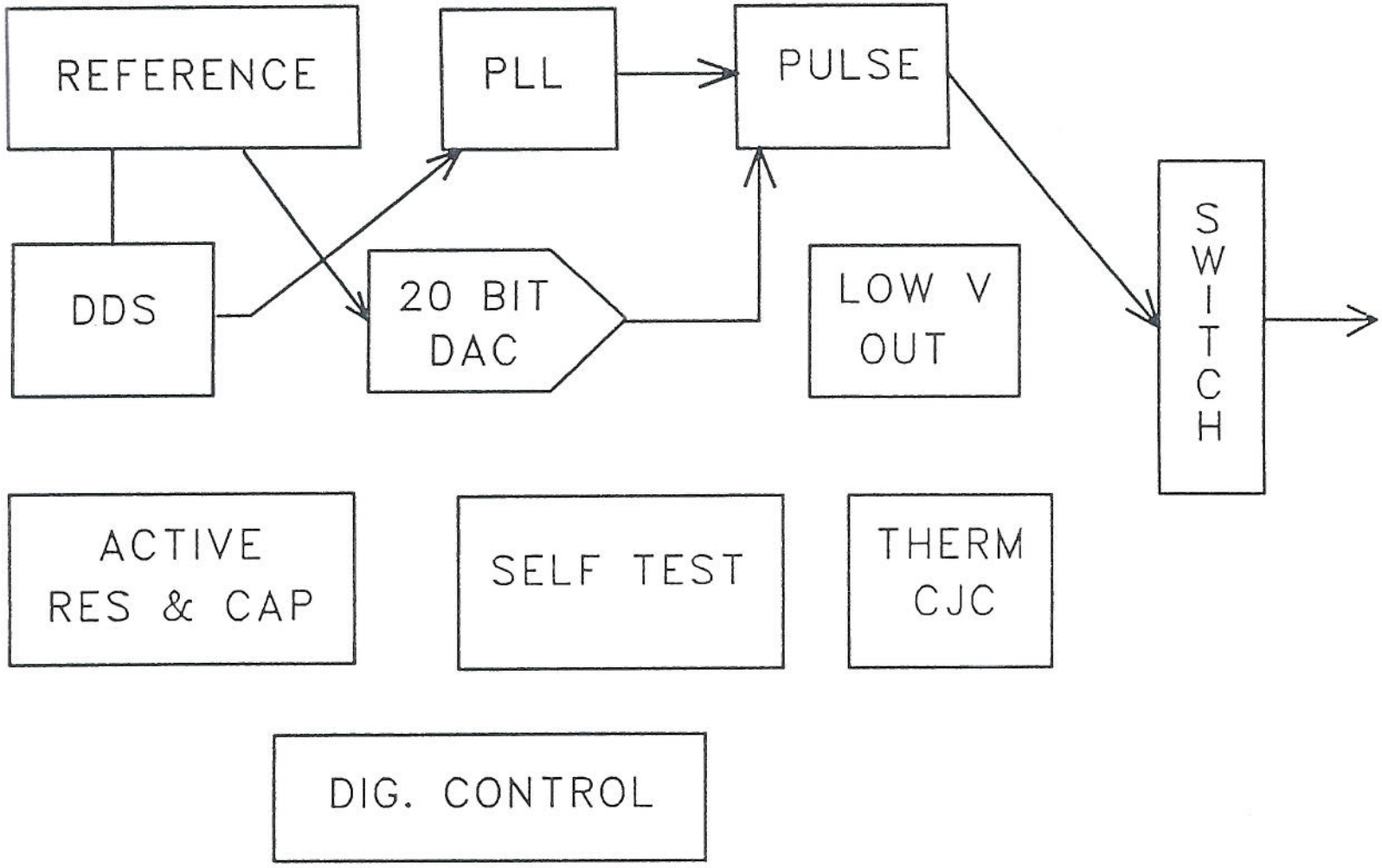
FUN1

C45



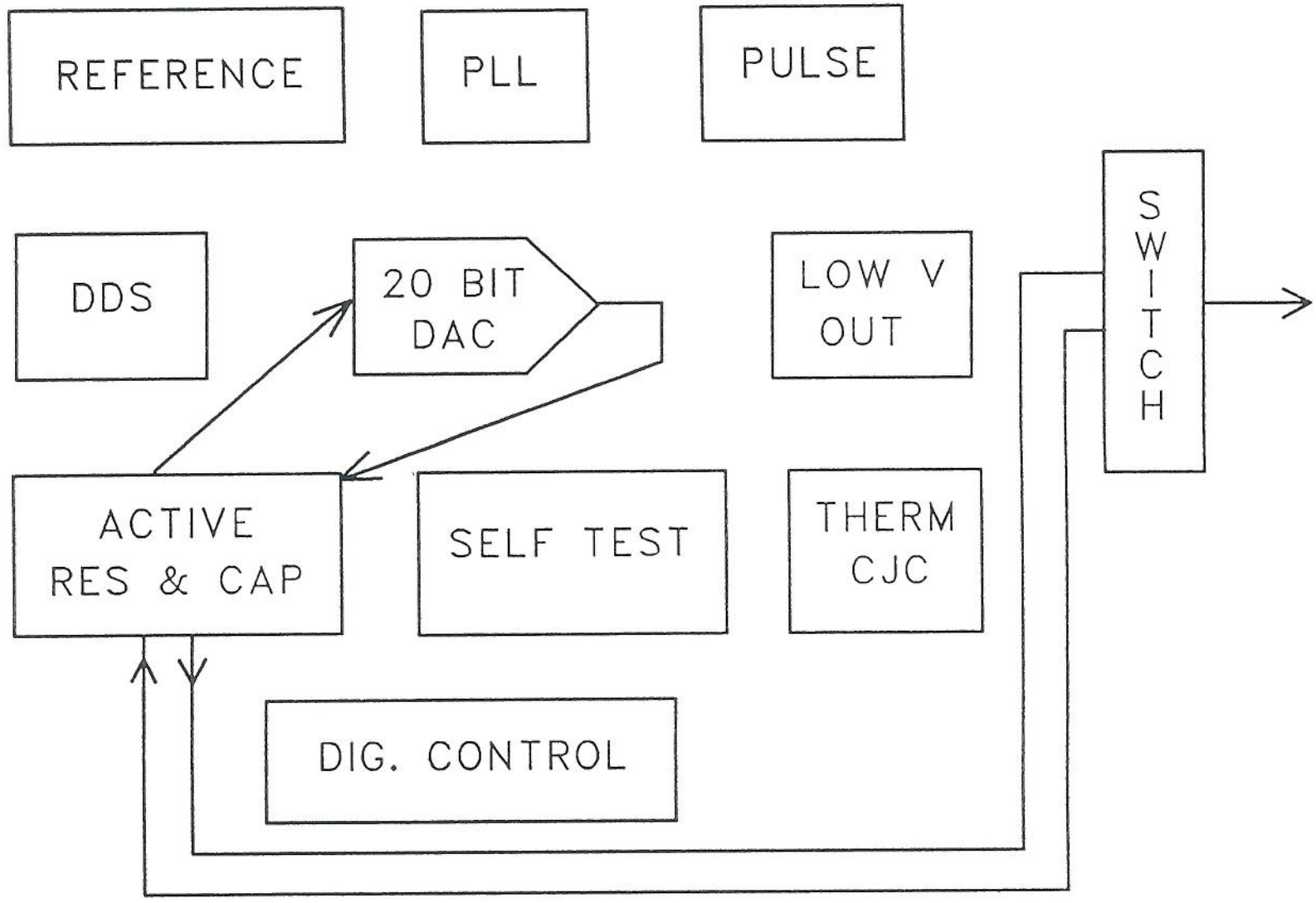
LOW VOLTS AC

FUN2


REFERENCE
PLL
PULSE
DDS
20 BIT DAC
LOW V OUT
SWITCH
ACTIVE RES & CAP
SELF TEST
THERM CJC
DIG. CONTROL

PULSE

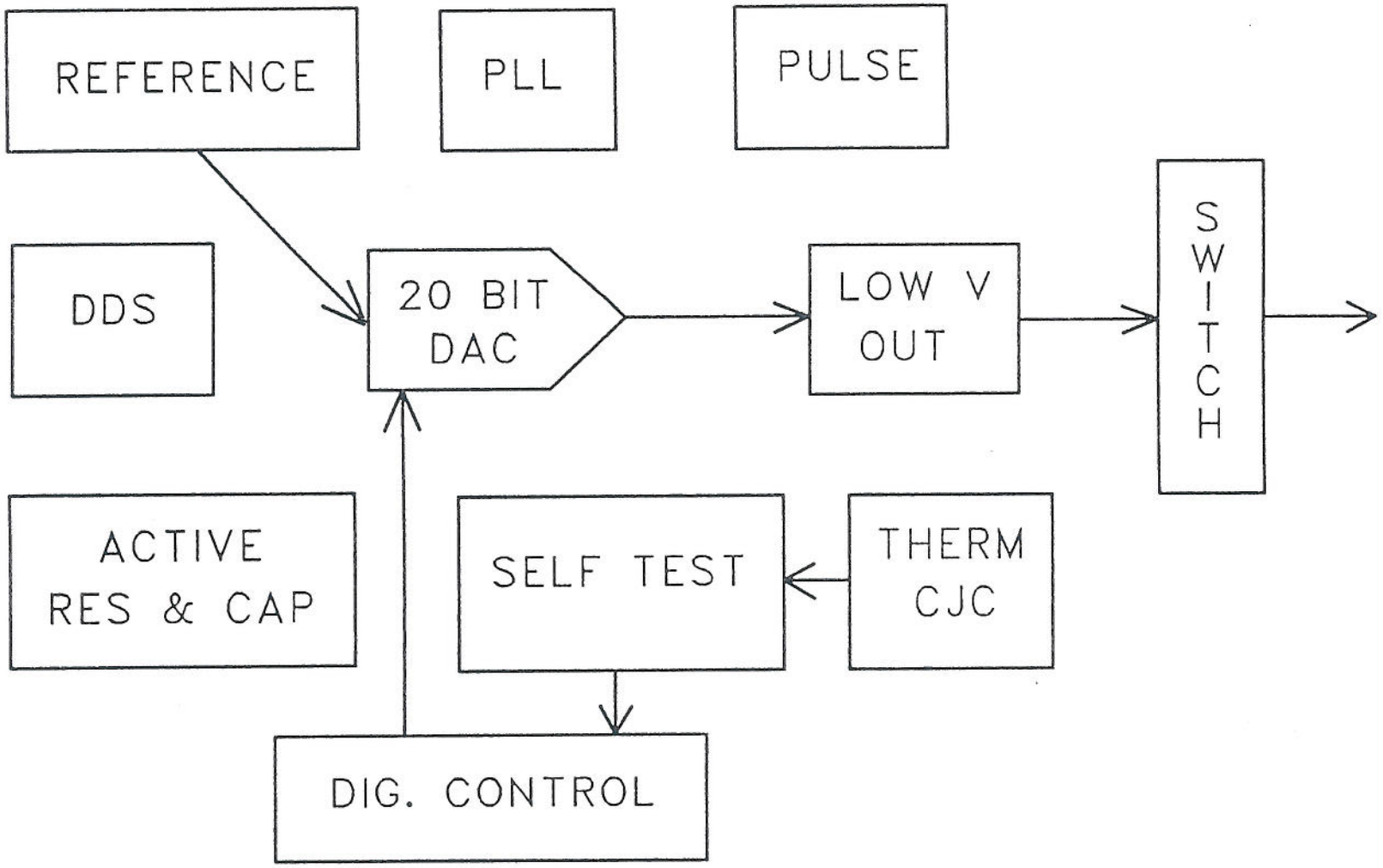
FUN3



ACTIVE Z

FUN4

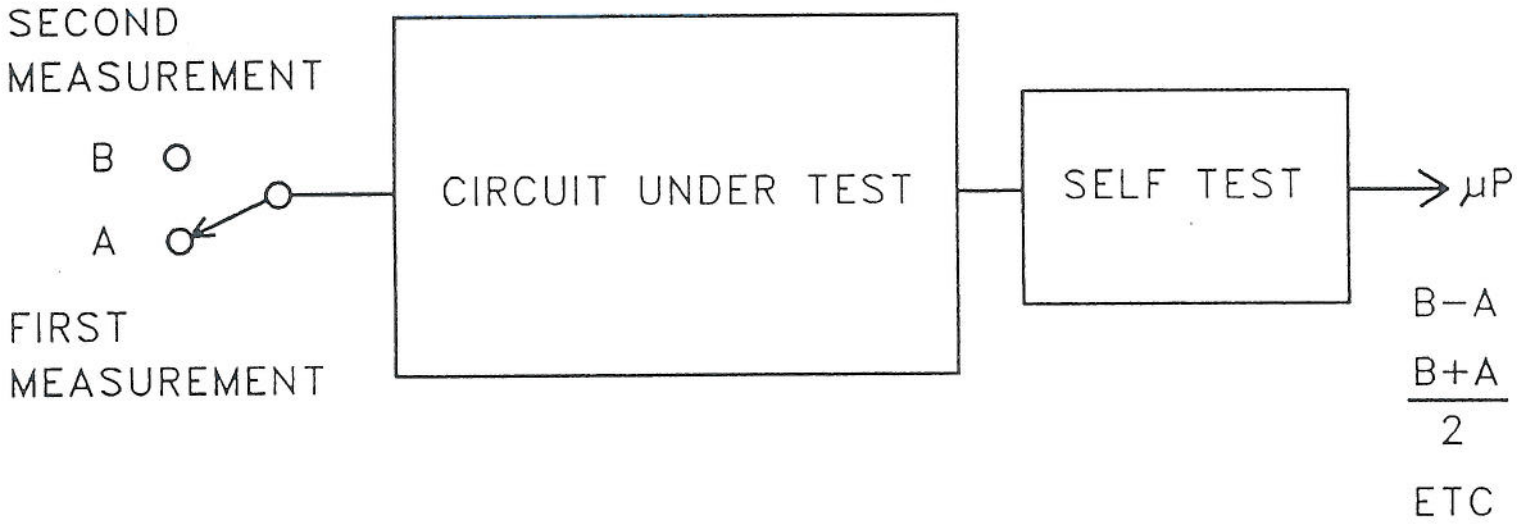
C48



THERMOCOUPLE

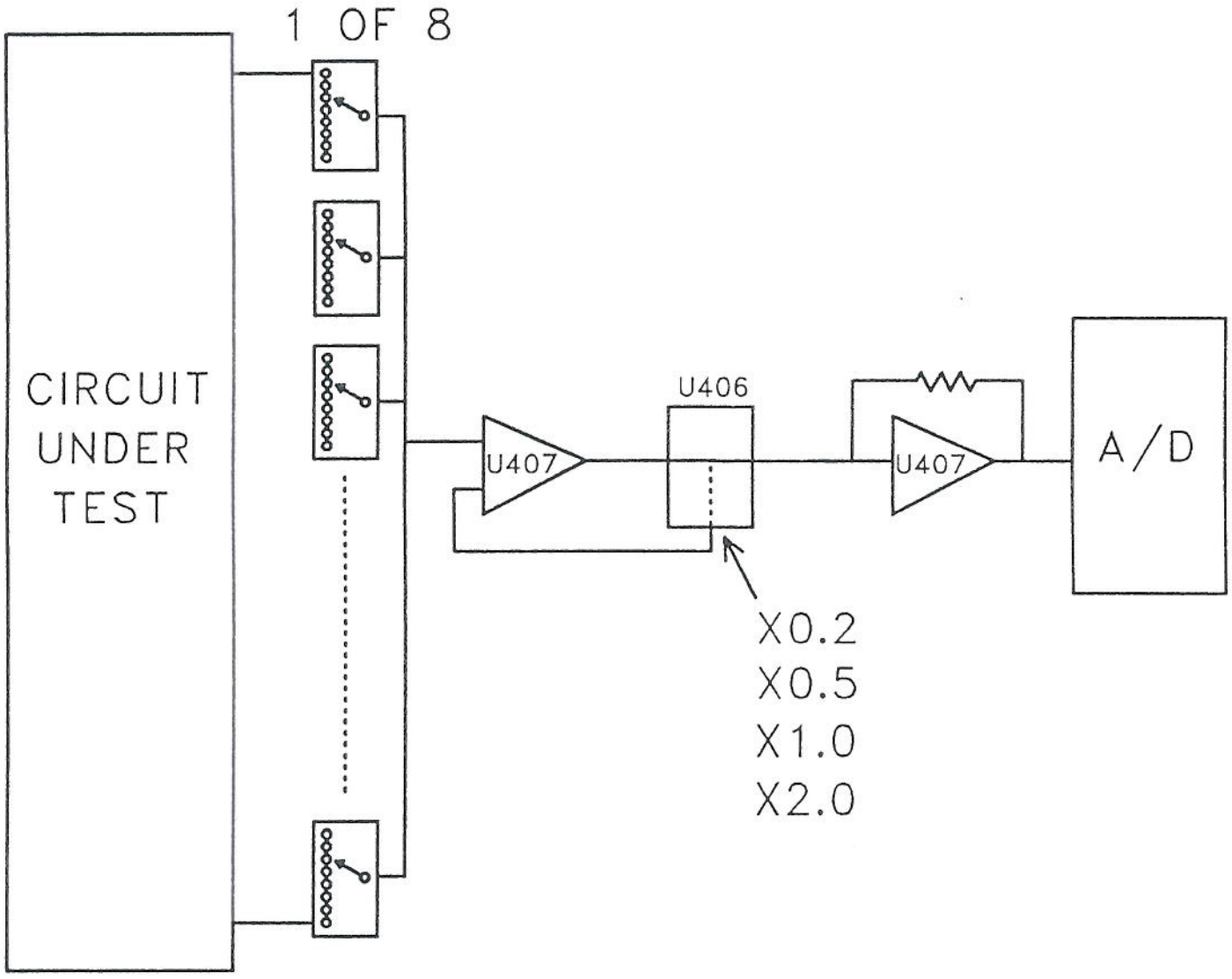
FUN5

C49

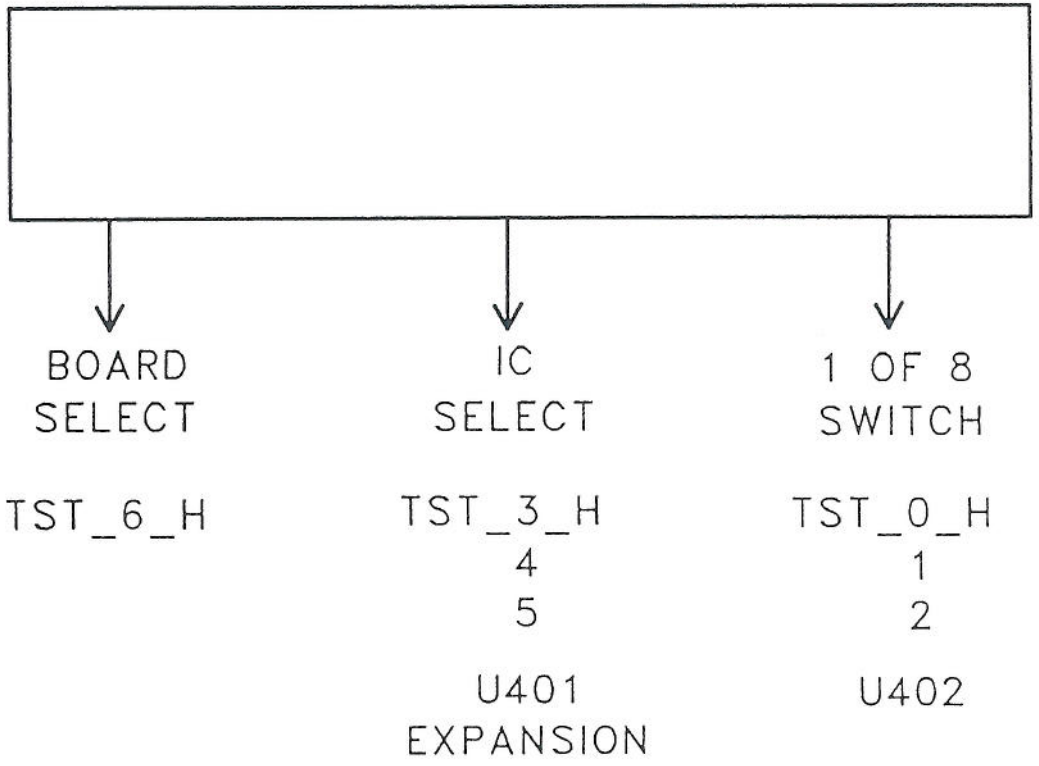


SELF TEST PRINCIPLE

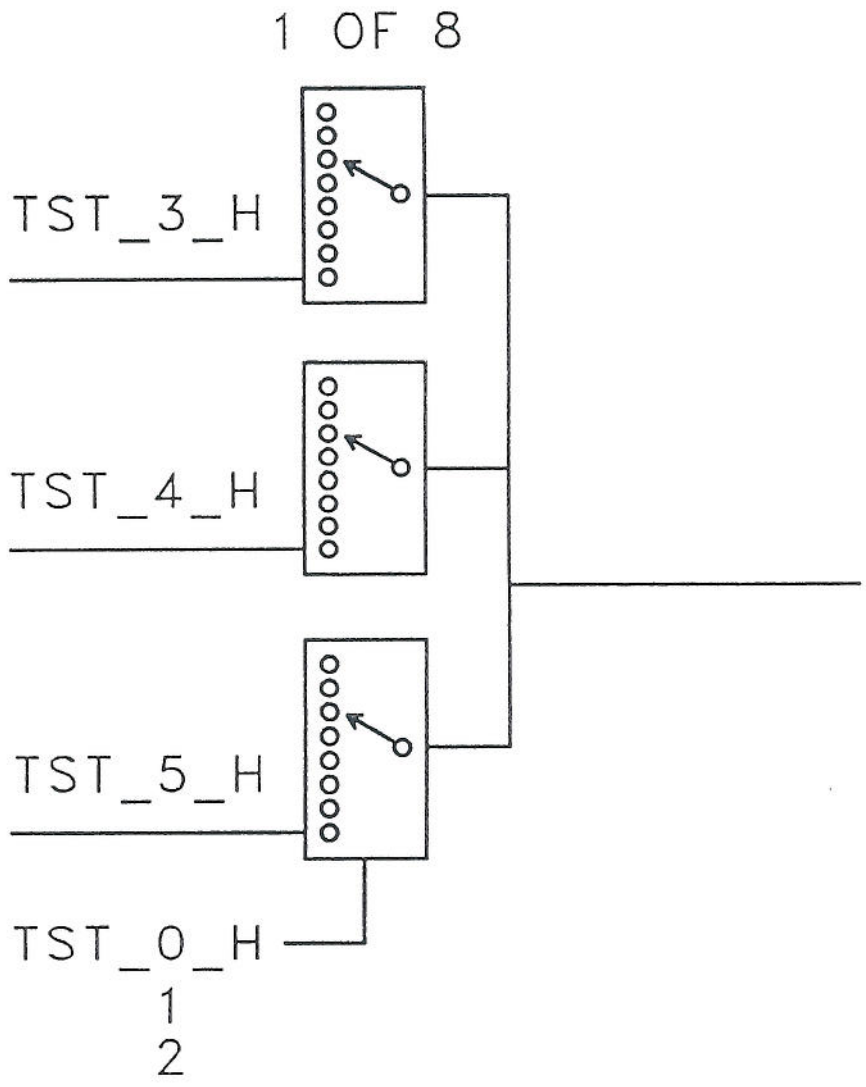
STO1



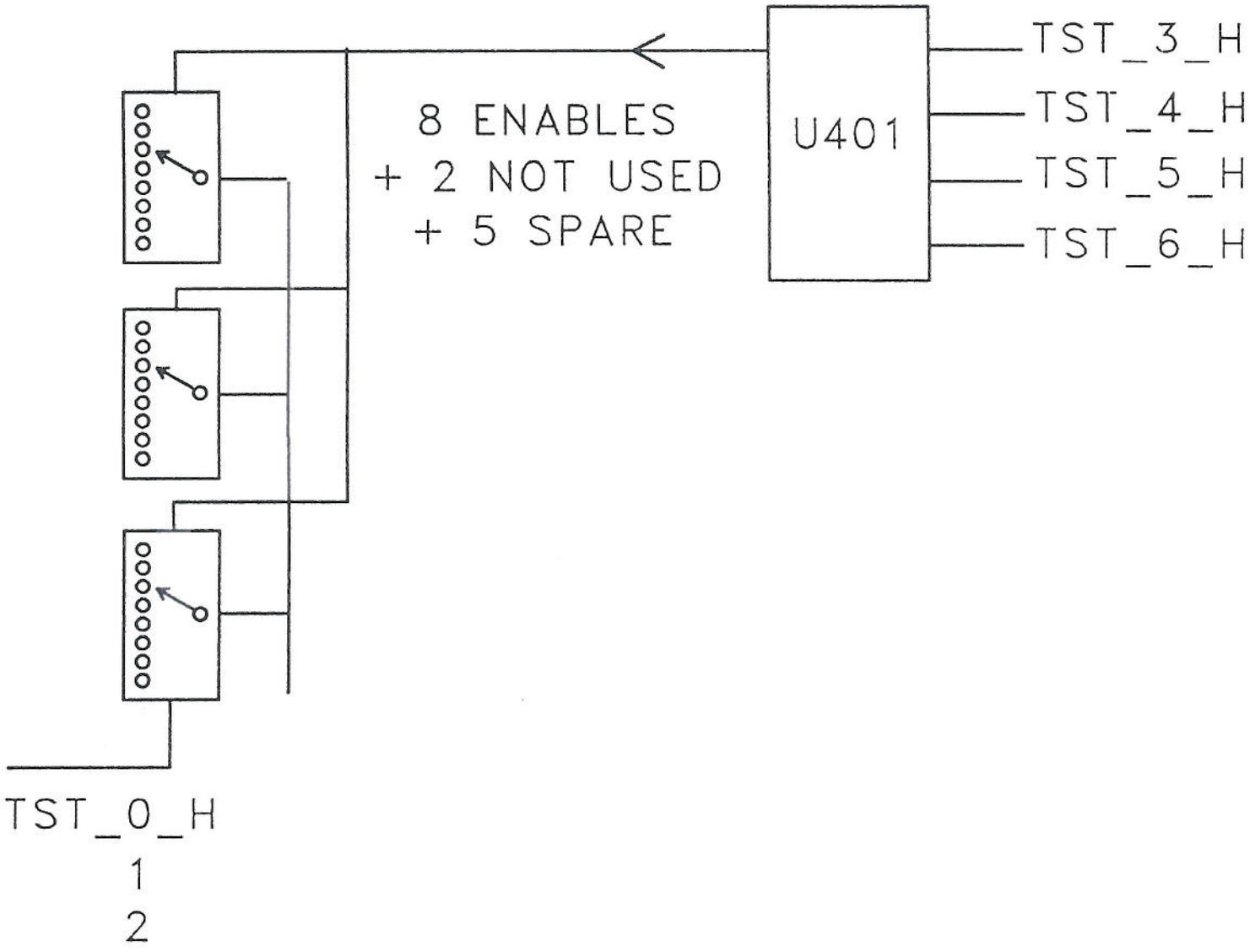
SELF TEST OVERVIEW



SELF TEST ADDRESSING



POWER BOARD SELF TEST



ANALOGUE BOARD SELF TEST

ANALOGUE PCB DIGITAL INTERFACE.

LINE	FUNCTION
AN_D0 to AN_D7 plus REG_D8 to REG_D27 (D12 - D15 not used)	These twenty four lines form the data bus to three DACs, U105, U106 and U107. U106 is the main DAC. U107 provides a gain trim of the main DAC with a span of 8 LSBs, with 4 bits overlap. Nominal Vref is 6.5536. The 4 bits of overlap is more than enough to cope with linearity errors in the main DAC. This gives a 20 bit DAC. U105 provides current tickle inputs or an offset trim for the 20 bit DAC.

NOTE. These lines are not unique to these devices.

DAC_REF_WR_L When Lo, writes data into U105.

DAC_MAIN_WR_L When Lo, writes 24 bits into U106 and U107.

DAC_REF_NEG_L When Lo, applies a negative reference voltage to the main 20 bit DAC. Used in DC volts functions only, to get a positive output. Default Lo.

DAC_DDS_DC_HV_H Selects i/p source to DDS DAC U114.
Lo connects REF_OUT direct to DDS. This is used for all functions except DCV HV. (In DCV LV the DDS is not actually active).
Hi connects DAC_OUT_1 to DDS. This is used for DCV HV only.
Default state is Lo.

DAC_DDS_H_REF_L Selects i/p source to 20 bit main DAC, via U116 and U106.
Lo connects REF_OUT direct to the DAC. This is used for DCV HV, DCV LV, FREQ, and PULSE.
Hi connects DDS o/p to the DAC. This is used for ACV LV and ACV HV.
Default state is Lo.

In summary:-

DAC_DDS_H_REF_L \ DAC_DDS_DC_HV_H	0	1
0	DCV LV FREQ,PULSE DEFAULT	DCV HV
1	ACV LV & HV	NOT USED

colin\dad65\doc\analbrd8
25 mar 1994

DAC_F1_H
DAC_F0_H

DAC_F1_H is the MSB. The main 20 bit DAC has four inputs and outputs, selected in U115 by means of these two control lines.
The input impedance is > than 1Mohm.
The output impedance of DAC_OUT_1 is very low.
The other o/p impedances are around 200ohms and should always be buffered.
DAC_OUT_4 is reserved for expansion functions.

DAC_F1_H \ DAC_F0_H	0	1
0	1 V/I Functions Default	2 Active Impedance
1	3 SPARE	4 Expansion Bus

MAIN DAC INPUT OUTPUT CONTROL

PLL_EN_L

When Lo the Phase Locked Loop U502, U503 commences to oscillate in a controlled fashion.
Default Hi.

PLL_R0_H
PLL_R1_H
PLL_R2_H

These control lines set the frequency band of the PLL and control the state of the current tickle into self test and cap. self cal.

FUNCTION	PLL_R2_H	PLL_R1_H	PLL_R0_H	CAP/I
200KHz-800KHz	0	0	1	1n267
800K01-3M2	0	1	1	267p
3M201 -12M8	1	1	1	47p
Tickle OFF	0	0	1	(DEFAULT)
Tickle HI I	0	1	0	218 uA
Tickle LO I	1	0	0	2.18uA

NOTE. The relay functions described below are hierarchal.

RL_OP_ON_H
Affects relays K008, K010.
Hi connects internal circuitry to terminals.
Lo isolates all internal circuitry except K301, (described later).
Default to Lo.

RL_HV_H_LV_RCG_EXP_L
Affects Relays K005, K006, K007.
When Hi, Power Amp (3v-1000v) is connected to the terminals.
When Lo, any other function is permitted.
Default to Lo.

RL_RCG_EXP_H_LV_L
Affects relays K002 and K004.
When Lo, Low Voltage Amp (<3v), or the Frequency/Pulse circuit may be connected to the output terminals if the relays above so permit. (See RL_FRQ_PLS_H_LV_L below)
When Hi, it permits all other functions except those requiring the Power Amp o/p. (See above)
Default to Lo.

RL_RCG_H_EXP_L
Affects relays K001, K003, U108/16,8
When Hi, the RCG (res, cap, cond,) circuit may be connected to the output terminals if the relays above so permit. The main DAC is offset corrected via U105 etc.
When Lo, the Expansion functions may be permitted, and the main DAC is given a fixed offset via R143.
This line is active even if no expansion function is actually fitted.
Default to Lo.

RL_FRQ_PLS_H_LV_L
Affects relay K303, and U508.
When Hi the Frequency/Pulse function may be connected to the output terminals if the relays above so permit.
When Lo, the Low Voltage Amp may be connected to the output terminals if the relays above so permit.
Default to Lo.
In addition to controlling the relay, U508 is also controlled so as to collapse the power rails of the Frequency/Pulse output stage, and to prevent comparator U501 from switching.

RL_LEXP_H_BEXP_L
Now a spare control line. Don't tell anyone!

NOTE. This is the end of the Hierarchal relay descriptions. However, subsequent descriptions will not necessarily be independent of the above relays.

EXP_ON_H — Affects relay K304. (Sourced from power brd.) This provides the facility for an expansion function to utilise the protected LV_P_HI output.
When H, the protection circuits can be connected round an expansion circuit TBD, which can be a measurement or generation circuit.
Default to Lo.

RL_TCPL_ON_H — Affects K012.
When Hi, the LV_P_HI and LV_P_LO outputs are connected directly to the thermocouple outputs.
When this facility is in use, RL_RCG_EXP_H_LV_L **must** be Hi or there will be an error.

UPD_H — Affects all relays.
When pulsed Hi, K008 and K010 have 30v across the coil if the output is required to be ON.
When held Lo, K008 and K010 if actives have 15v across the coil to hold the contact. If inactive they have 15v across the coil in the opposite direction. Thus the O/P relays are effectively in constant power mode.
All other relays are latching types, and receive a pulse of current to set or reset them when UPD_H is pulsed.
Default to Lo.

V_3V+3MA+300MA_L
When Lo in DC or AC volts, selects R901 tap for the 3v range. When Lo in DC or AC current, selects input volts for 3mA and 300mA ranges.
Default Hi.

V_300MV+30MA+3A+20A_L
When Lo in DC or AC volts, selects R901 tap for the 300mv range. When Lo in DC or AC current, selects input volts for 30mA, 3A and 20A ranges.
Default Lo.

Note. In the two control lines above, one must be Hi and the other Lo at all times.

DDS_SMPL_L — A Hardware function only active with DDS. A pulsed low waveform, nominally at 1.2MHz, with the lo mark being 120nsec in the first instance. Liable to change as part of the optimisation process.

SELF TEST INTERFACE

TST_6_H — Hi selects power board, Lo selects analogue board and expansion board. Default Hi.

TST_5_H, TST_4_H, TST_3_H — If TST_6_H is Lo, TST_5_H is the MSB. In this case, the three lines are decoded to give values 0-7. Values 0,1,2 enable U402, 403, 404 respectively, on the analogue board. The remaining values are available for expansion purposes.
If TST_6_H is Hi, the three lines become direct enables with no decoding or expansion facility. On the power board only:-
TST_5_H enables U506 when Hi. Default Lo.
TST_4_H enables U406 when Hi. Default Hi.
TST_3_H enables U307 when Hi. Default Lo.

NOTE. TST_6_H to TST_3_H are sourced on the power board.

TST_2_H, TST_1_H, TST_0_H — TST_2_H is the MSB. The component enabled as described above is an 8:1 multiplexing device. The address of the required input, 0-7, is set by these three lines.
Default to Hi, Hi, Hi, address=7.

ADC_R0_H, ADC_R1_H — Self Test has four gain settings selected as follows:-

ADC_R0_H

ADC_R1_H	0	1
0	x 0.2 Default	x 0.5
1	x 1.0	x 2.0

NOTE. The maximum voltage AFTER the gain factor above has been applied should be +/-2.5 volts to ensure the A/D reads within its scale.

ADC_CONV_H — If pulsed Hi, the A/D will perform one conversion. If held high, conversions would be

continuous, but hardware precludes this.

ADC_CAL_H — If Hi prior to or synchronous with ADC_CONV_H becoming Hi, the A/D self calibrates itself in gain and offset, relative to its reference i/p and its internal zero. Inputs are ignored.

TST_ACV_L — **DELETED.** Configures OP_SLFTST. When Lo, a simple filter, C902 is in circuit.

TST_ATN_L — **DELETED.** Configures OP_SLFTST. When Lo, an attenuation of 110:1 is present between LV_P_HI and OP_SLFTST.

NOTE. The following descriptions refer to the Resistance, Conductance and Capacitance functions.

EN_LDCOMP_H — Hi enables the Lead Impedance compensation circuit. This is independent of the user. K302 is enabled, and U306 controlled.

RL_EN_CUST_2W_H — Under customer control. As two or four wires may be connected to the terminals, the customer is prompted to tell us the current state. If there are only two wires, this line is driven Hi, which makes K301, giving a local sense facility at the terminals of our machine. Otherwise, left Lo.

3EN_H, 3A2, 3A1, 3A0 — These lines control the selection of the impedance defining the I/V gain of U605. 3EN_H and its derived line 3EN_L enable U602 and U603 or U604. The others select one switch from the enabled pack. Several FETs are also controlled, making a low leakage switch.

2A2, 2A1, 2A0 — The MSB 2A2 is derived from (1A1 AND 1A0). The lines select Zset, part of R648, by means of U610 and U611.

1A1, 1A0 — These lines select Zstd, part of R648 or 10u, by means of U609.

OHMS RANGE SELECTION

RANGE	EN_L DCOMP_H	3EN_H	3A2	3A1	3A0	2A1	2A0	1A1	1A0	Zin	Zset	Zstd
0-40R	1	1	1	1	1	1	0	0	0	2K85	200K	2K85
Hi 40 -400R	1	1	1	1	1	0	1	0	0	2K85	20K	2K85
Li 40 -400R	1	1	1	1	0	1	0	0	0	28K5	200K	2K85
Hi 400 -4K	1	1	1	1	1	0	1	0	1	2K85	20K	28K5
Li 400 -4K	1	1	1	1	0	0	1	0	0	28K5	20K	2K85
Hi 4K -40K	1	1	1	1	0	0	1	0	1	28K5	20K	28K5
Li 4K -40K	1	1	1	0	1	0	1	0	0	285K	20K	2K85
Hi 40K -400K	1	1	1	0	1	0	1	0	1	285K	20K	28K5
Li 40K -400K	1	0	1	0	0	0	1	0	0	2M85	20K	2K85
Hi 400K -4M	0	0	1	0	0	0	1	0	1	2M85	20K	28K5
Li 400K -4M	0	0	0	0	1	0	1	0	0	28M5	20K	2K85
Hi 4M -40M	0	0	0	0	1	0	1	0	1	28M5	20K	28K5
Li 4M -40M	0	0	0	1	0	0	1	0	0	285M	20K	2K85
Hi 40M -400M	0	0	0	0	1	0	1	1	0	28M5	20K	285K
Li 40M -400M	0	0	0	1	0	0	1	0	1	285M	20K	28K5

CAPACITANCE RANGE SWITCHING

RANGE	EN_L DCOMP_H	3EN	3A2	3A1	3A0	2A1	2A0	1A1	1A0	Zin	Zset	Zstd
500p-4n0	0	0	0	1	1	1	1	0	1	1n8	6K35	28K5
4n0-40n	0	1	0	0	1	1	1	0	1	15n	6K35	28K5
40n-400n	0	1	0	1	0	1	1	0	1	147n	6K35	28K5
400n-4u0	1	1	0	1	1	1	1	0	1	1u5	6K35	28K5
4u0-40u	1	1	0	0	0	1	1	0	1	10u	6K35	28K5
40u-400u	1	1	1	1	1	1	0	1	1	2K85	7K00	10u
400u-4mF0	1	1	1	1	1	0	1	1	1	2K85	70K0	10u
4mF0-40mF	1	1	1	1	1	0	0	1	1	2K85	700K	10u

POWER PCB CONTROL BITS – VOLTAGE SECTION

SHT 1

HV_DC_H High for DCV 300/1000V ranges.
Connects high-voltage error amp output to control amp input.
Connects precision HV atten to error amp inverting input
Disconnects non-precision AC HV inner loop attenuator from error amp inverting input.
Disconnects local feedback resistor round error amp, allowing its use as high gain integrator.

AC_HF_H High on 300/1KVAC when freq > 3kHz
Increases bandwidth of inner ACHV loop for the HF transformer.

HV_DC_L Low for DCV 300/1KV ranges
Connects reference input to error amp non-inverting input.

HV_AC_L Low for ACV 300/1KV ranges
Connects VCA output signal to error amp non-inverting input.

HV_IP_ON_H High when output ON.
When low, saturates mean-sensi loop error integrator U108, ensuring undershoot at turn-on.

SHT 2

HV_IP_ON_H High when output ON.
When low, shuts down main voltage amplifier by starving discrete stages of current

HV_AC_L Low on 300/1KVAC ranges.
Connects output of HVAC error amp to main amplifier input.

EXP_ON_H/L These lines make the main amplifier inverting input available on the analog expansion bus, with or without R247 attenuator connected

DET_I_LO/HI_L Set the sensitivity of the overcurrent detector:-

DET_I_ LO	DET_I_ HI	DETECTOR SENSITIVITY	RANGES USED
Ø	1	HIGH	30VAC/DC, 100VAC
1	Ø	LOW	300AC(HF., ALL 1KV
1	1	MEDIUM	300DC, 300AC(LF)

PA_OL_L Goes low when overcurrent detector trips. Initiates software shutdown to neutral state. Gives user message "Overload of power amp"

SHT 5

HV_PS_ON_H High in 100VAC and all 1KV ranges
Operates ±200V switches Q505/508 to raise power amp supplies from ±70V to ±200V.

HV_PS_OL_L Goes low when current drawn from ±200V rails exceeds approx 200mA (average). Gives message "Overload of HV power supply"

LCD_BL_ON_L High when in standby.
When high disables the 12V regulator for the LCD backlight inverter.

RELAY CONTROL BITS – VOLTAGE SECTION

30+300V (K201) Lowers the value of four W/W resistors in P/A for operation on ±70V

100+1KV (K202/K109) K202 configures R247 P/A attenuator for 105V full scale.
K109 configures inner and outer loop HV attenuators for 1KV operation.

300+1KV (K102) Routes P/A output via step up transformers rather than direct to output.

HV_DC (K104/K105) K104 partially configures HF transformer secondaries to drive DCHV diode doubler/filter. K105 connects output of filter to PHI and completes configuration of HFTX secondary.

HV_NEG (K106) Reverses the output polarity of the diode doubler for negative outputs on 300/1KV DC ranges.

TX_HF (K103) When unenergised the P/A output connects to LFTX primary and when energised to HFTX primary. (300V/1KV ranges)

Slides for 9000 service presentation

A1. General layout - user interfaces and digital assy.
A2. Display - waveforms.
A3. Bezel assy. - keyboard - PCB arrangement and matrix.
A4. Bezel assy. - rotary encoder - waveforms.
A5. Interconnection assy. - simplified protection - new version.
A6. Memory card assy. - text explaining capabilities.

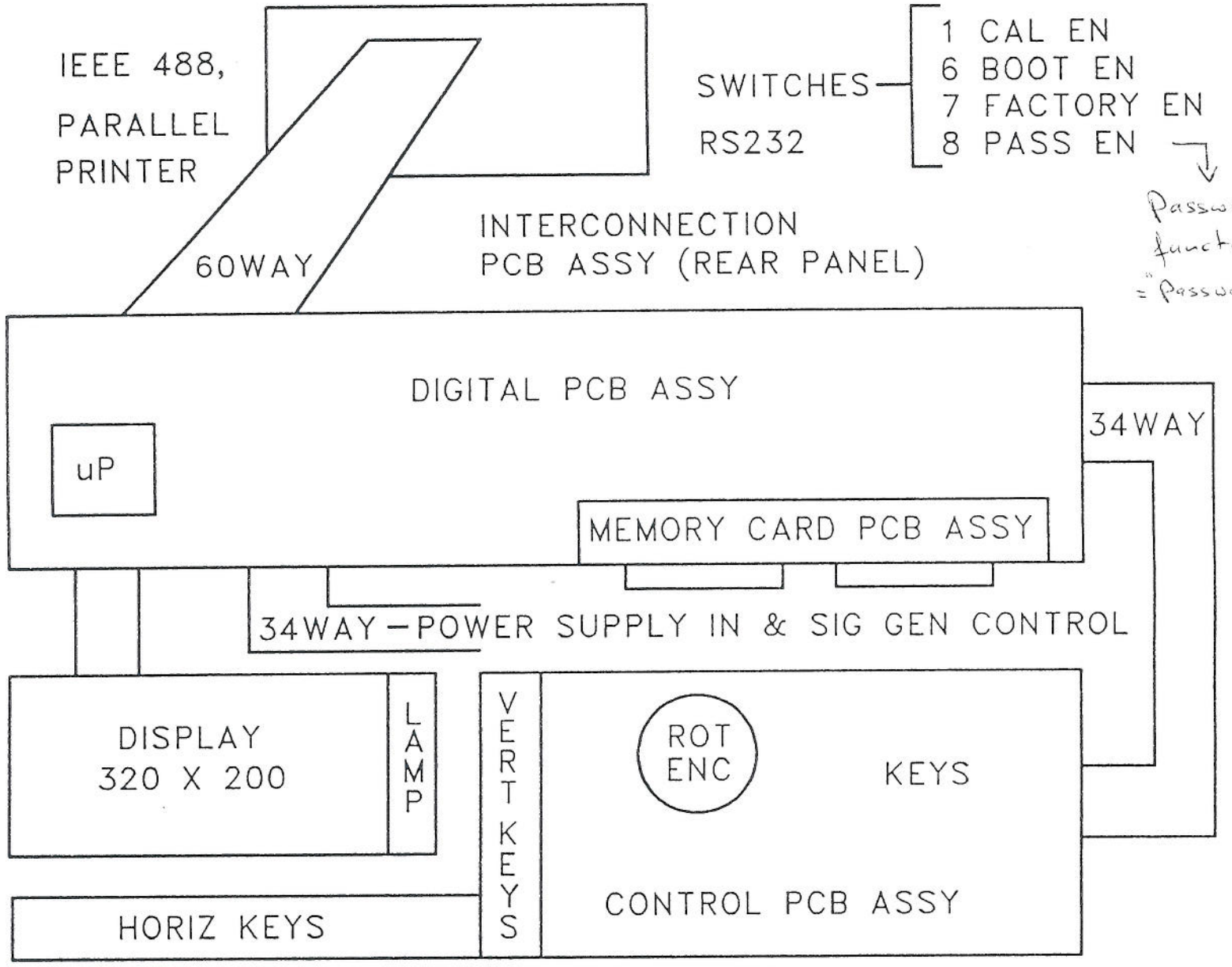
Digital assy:-
A7. Processor and memory.
A8. Clock generator, signal generation and display access time-out.
A9. LCD controller.
A10. Digital assy. power supplies.
A11. Keyboard encoder..
A12. Rotary encoder interface and bezel interrupts.
A13. Memory card interface.
A14. Signal generation parallel interface.
A15. IEEE 488 interface.
A16. RS232 interface.
A17. Parallel printer interface.
A18. Switches and boot mode.
A19. Reset and watchdog.

A20. Signal generation control interface - block diagram.
A21. Interface to signal generation circuits - description.
A22. Interface to signal generation circuits - waveforms.
A23. Power assy. - control registers in Actel.
A24. Analog assy. - control registers outside and in Actel.
A25. Analog assy. - control DACs.
A26. Analog assy - U701 internals - pulse counter and pulse/frequency selection.
A27. Analog assy - DDS digital.
A28. Analog assy - ADC interface.
A29. Power and analog assys. - detectors and counter time-out.
A30. Power and analog assys. - off key interlock and counter time-out.
A31. Power, analog and bezel assys. - On LED and Off key interlock enable.

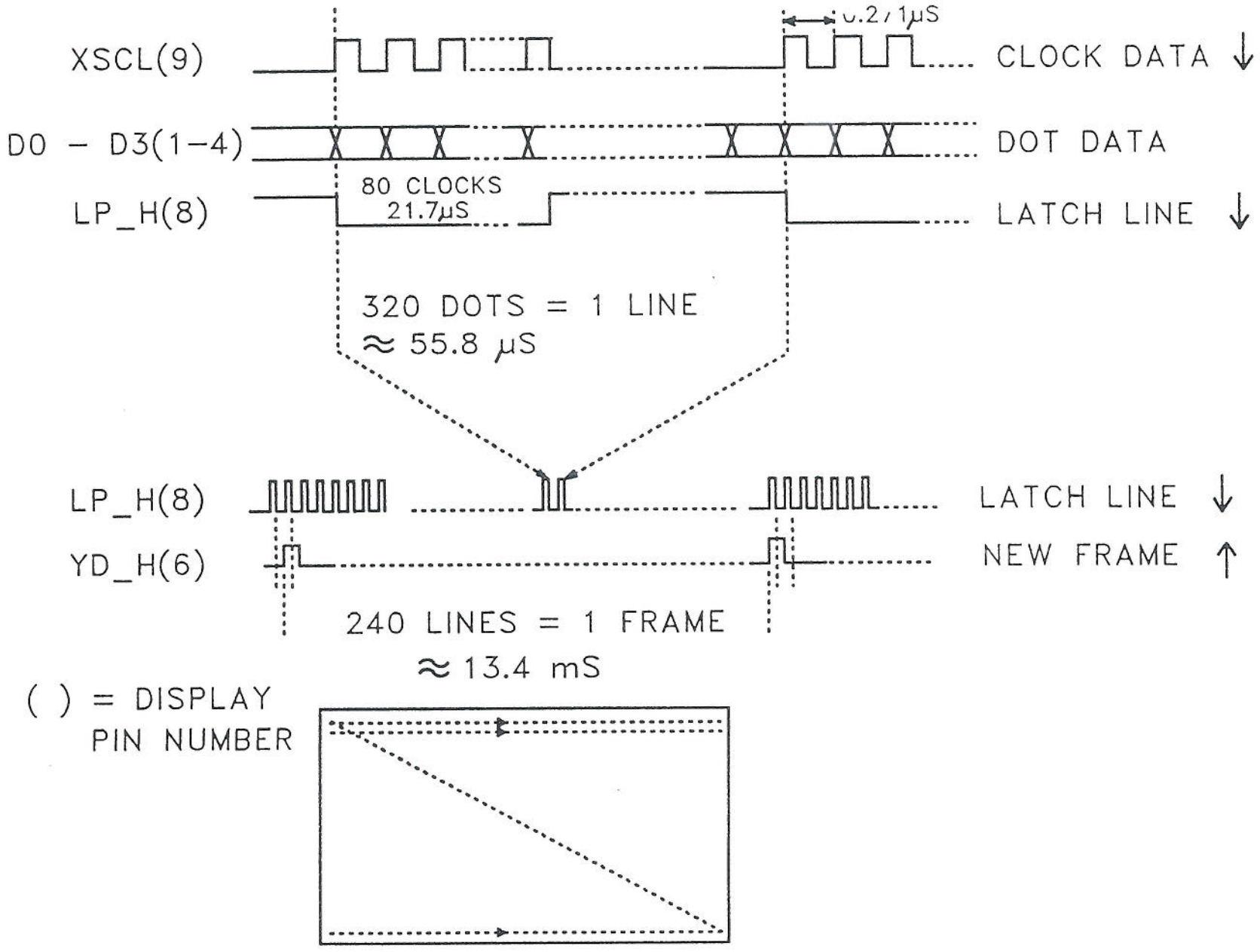
Not slides.
A32/33. Address decoding - digital assy.
A34/35. Address decoding - signal generation.
A36-41. Control bit sequence diagrams sheets.
A42. Digital fault finding - Model 9000

Software overview:-

Neutral state which most transition go through.
No state changes until output on sequences. No range selection with output off.
Internal state changes occur during self test and capacitance self calibration.
Signal generation interrupt and firmware detector off sequence to neutral.
Update pulse occurs when all control bits change. Jammed on if time-out occurs.

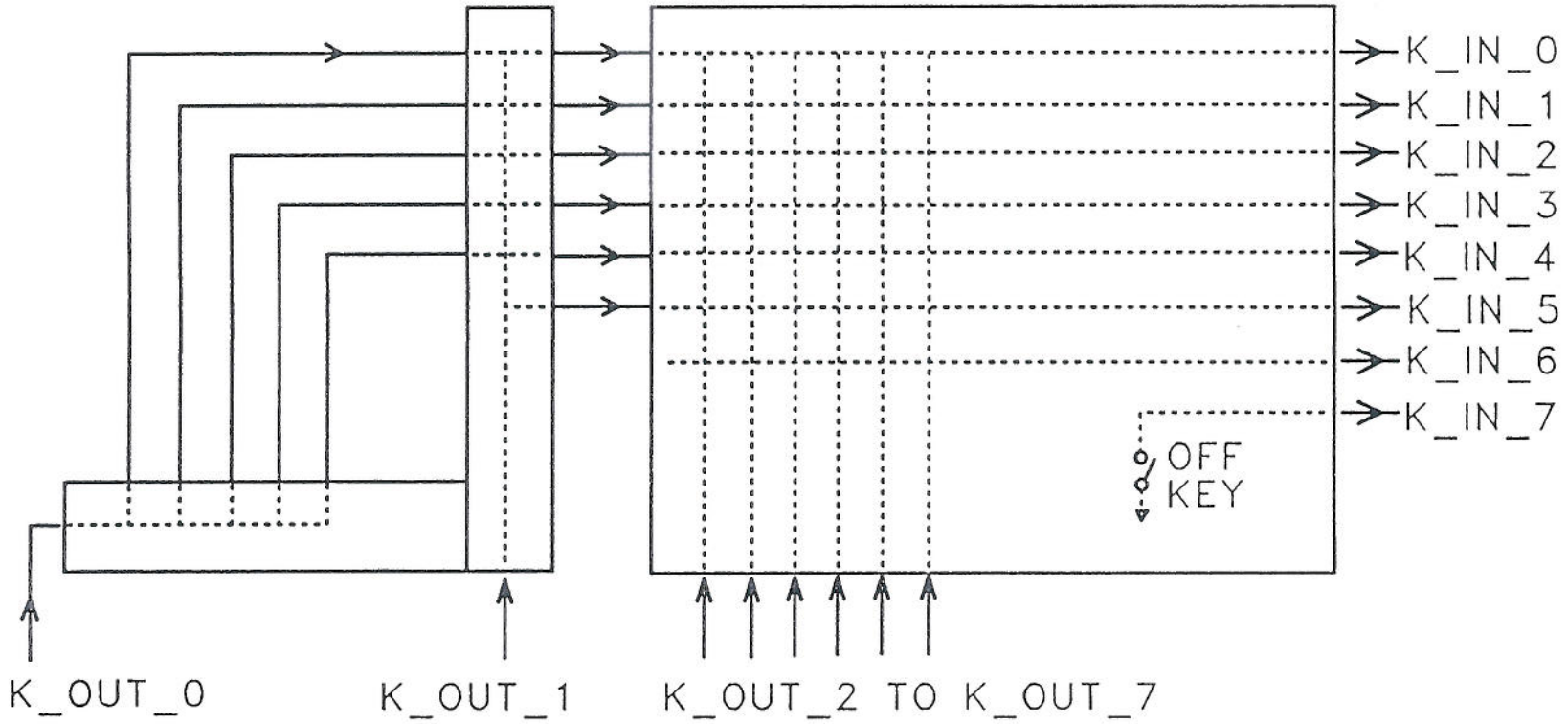


USER INTERFACES & DIGITAL PCB ASSY

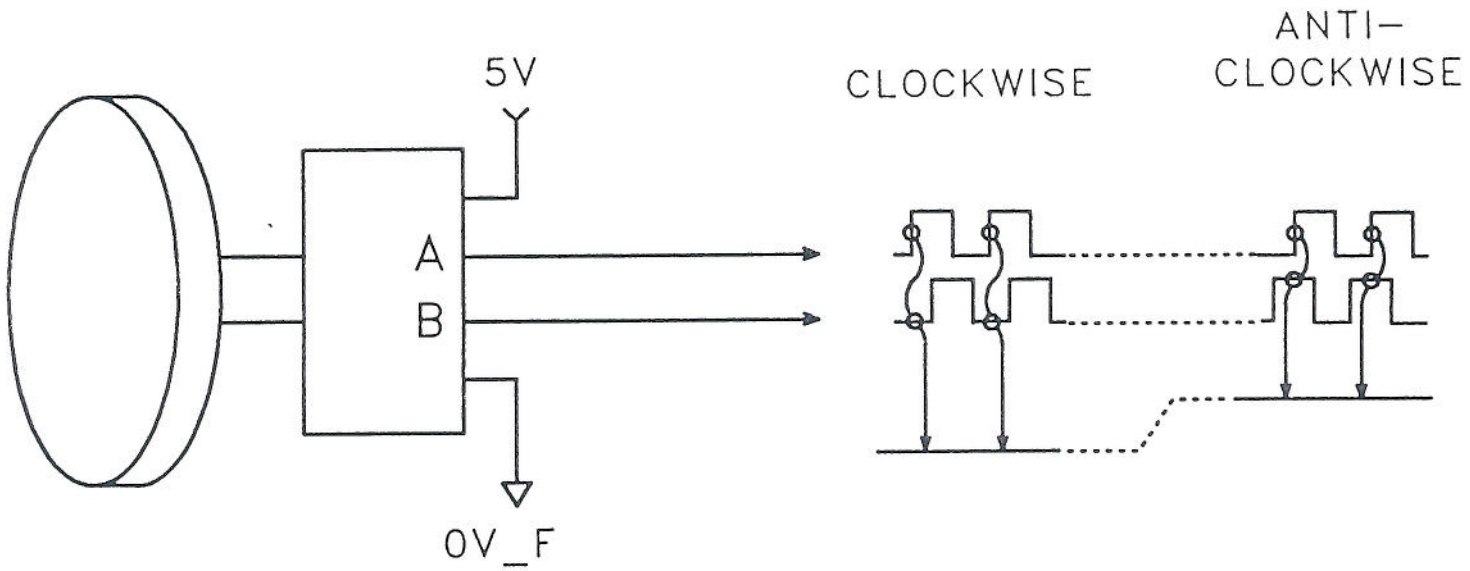


DISPLAY WAVEFORMS FROM CONTROLLER

1. KEYS ARE SCANNED IN AN 8X8 MATRIX.
2. KEY DESIGNATORS ARE CODED WITH DRIVE & SENSE LINES.
   e.g. S140 IS DRIVEN BY K_OUT_4 & SENSED BY K_IN_0

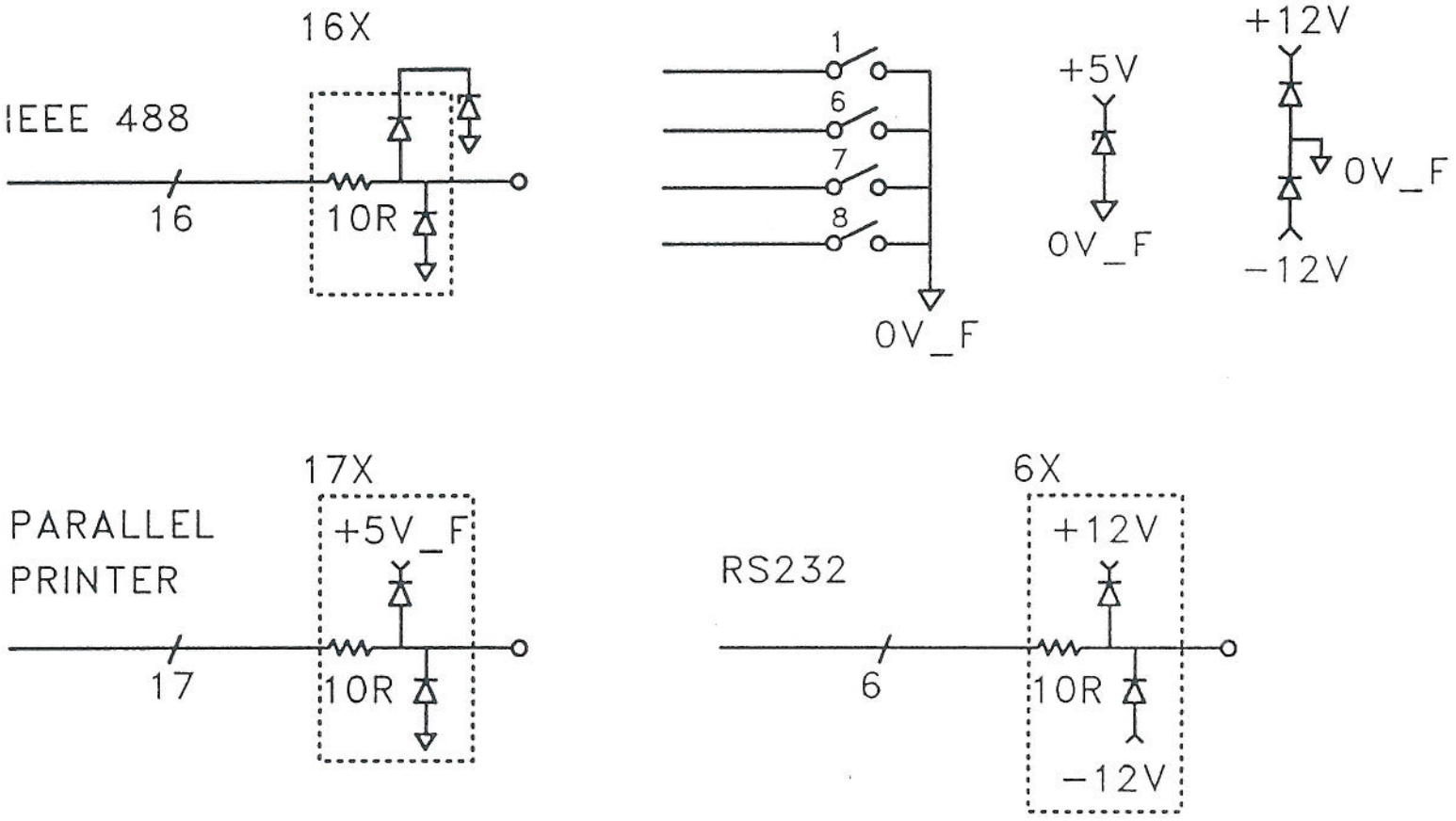


BEZEL ASSY – KEYBOARD



1. TWO CHANNEL OPTICAL ENCODER.
2. 64 LOGIC LEVEL PULSES PER REV.

BEZEL ASSY – ROTARY ENCODER



INTERCONNECTION ASSY

1. SUPPORTS TWO 68PIN CARD SOCKETS.
2. CONNECTS ADDRESS & DATA TO EACH SOCKET.
3. DRIVES EACH SOCKET WITH:

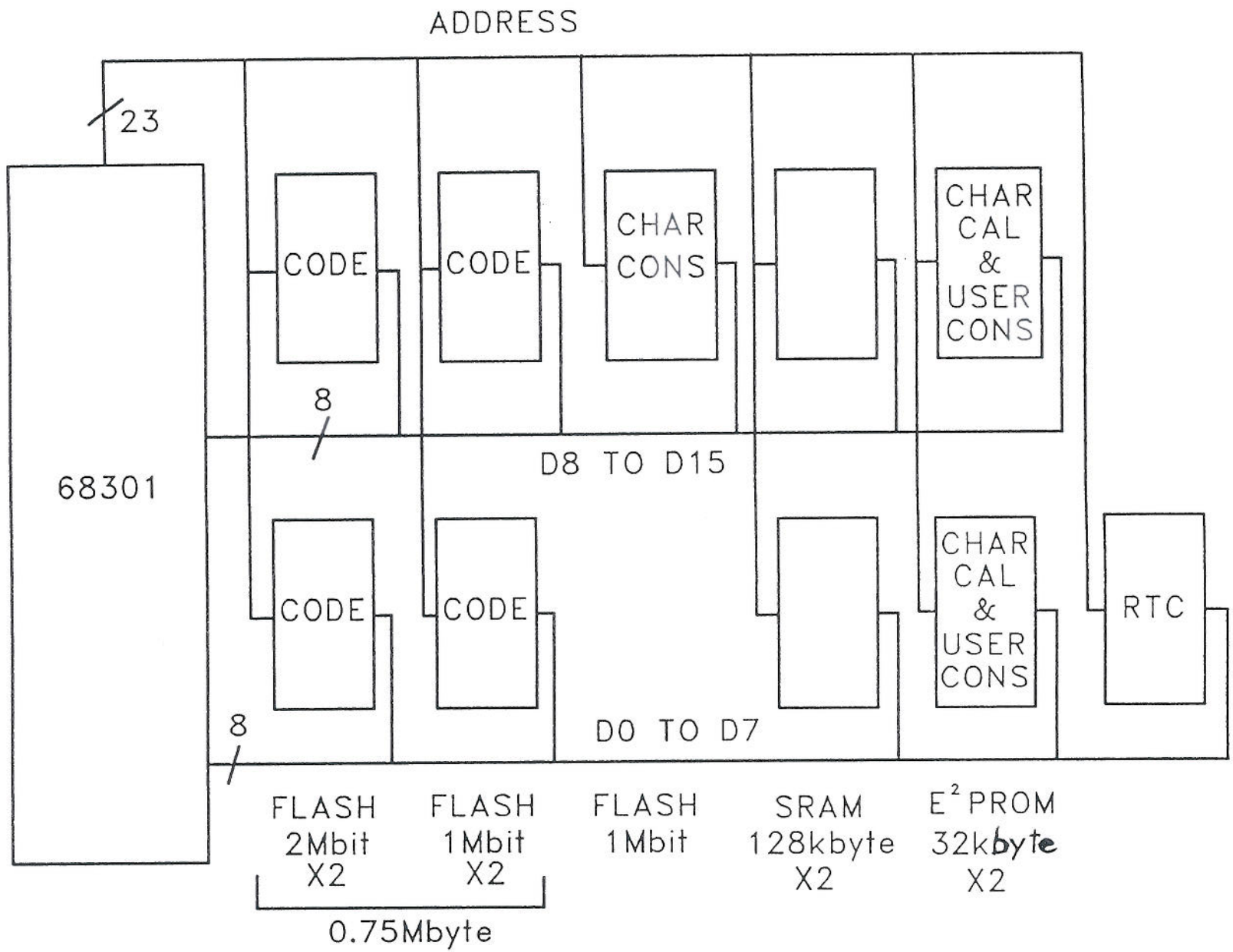
   CE1_L – LOW BYTE
   CE2_L – HIGH BYTE
   WE_L – WRITE DATA
   RD_L – READ DATA

4. RECEIVES ON EACH SOCKET:

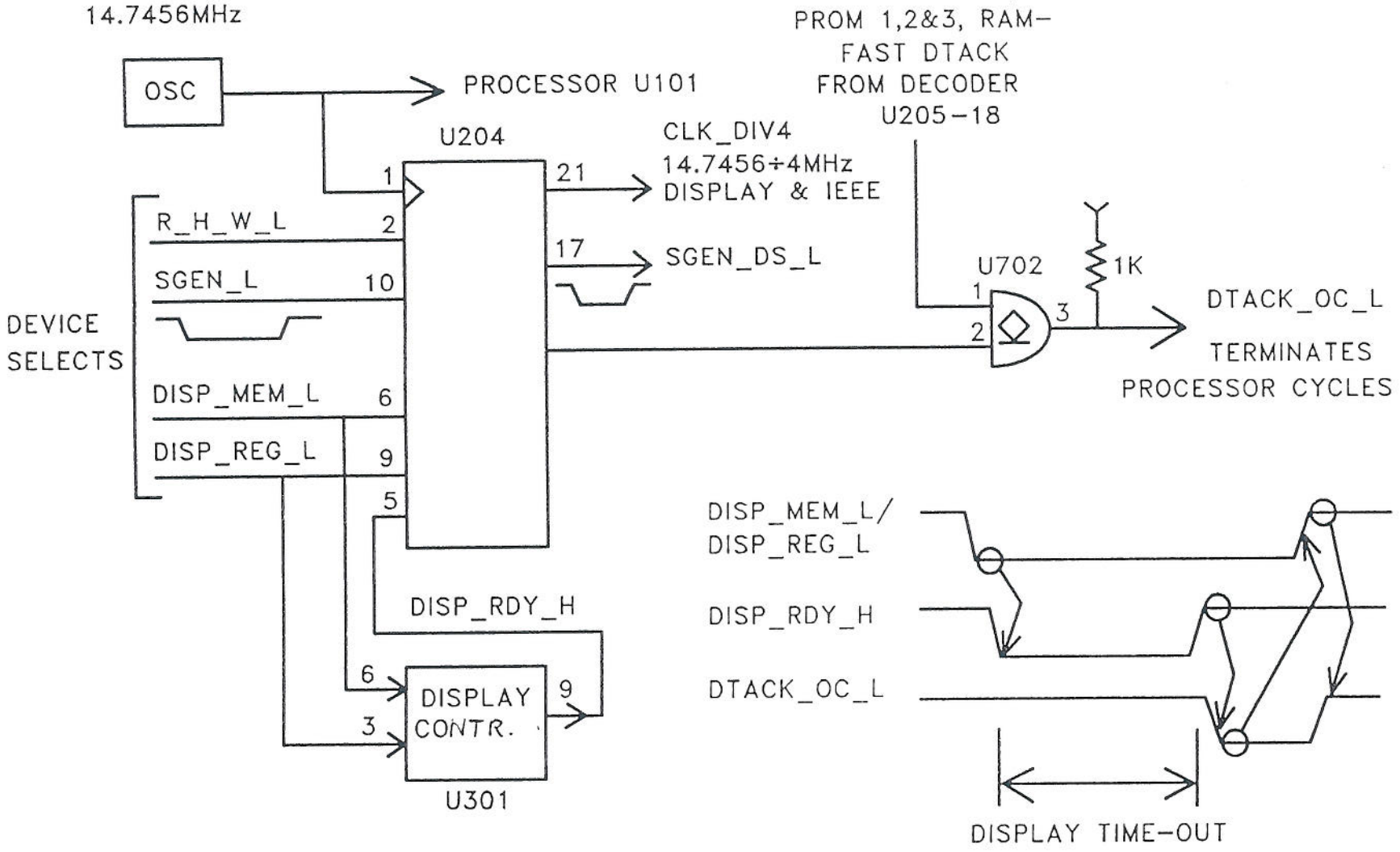
   CD1_L – CARD INSERTED
   CD2_L – CARD INSERTED
   WP_H – CARD WRITE PROT.
   BVD1_L – CARD BATTERY LOW
   BVD2_L – CARD BATTERY DEAD

5. SOCKET PINS SEQUENCE SUPPLIES & SIGNALS DURING INSERTION.

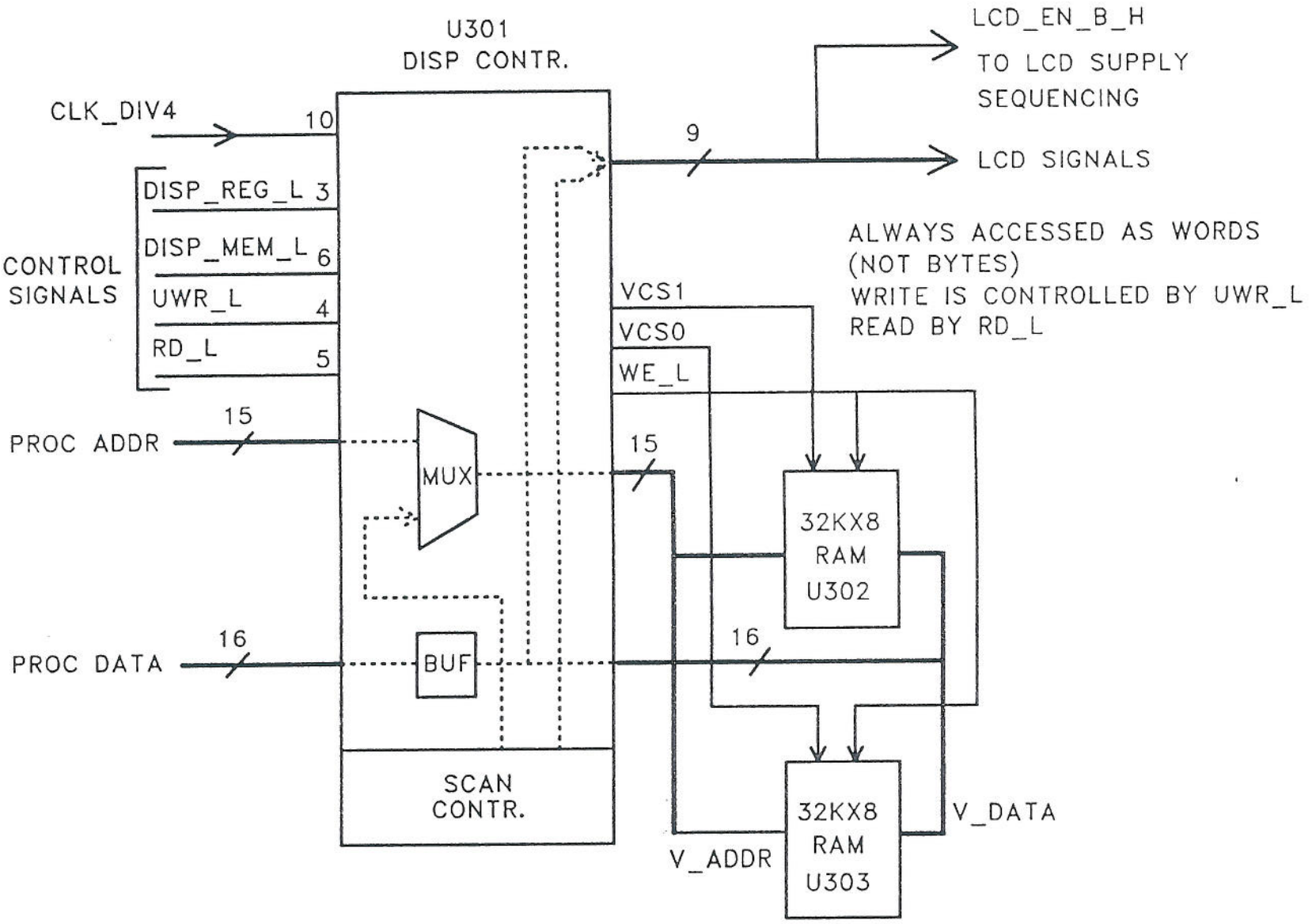
MEMORY CARD ASSY



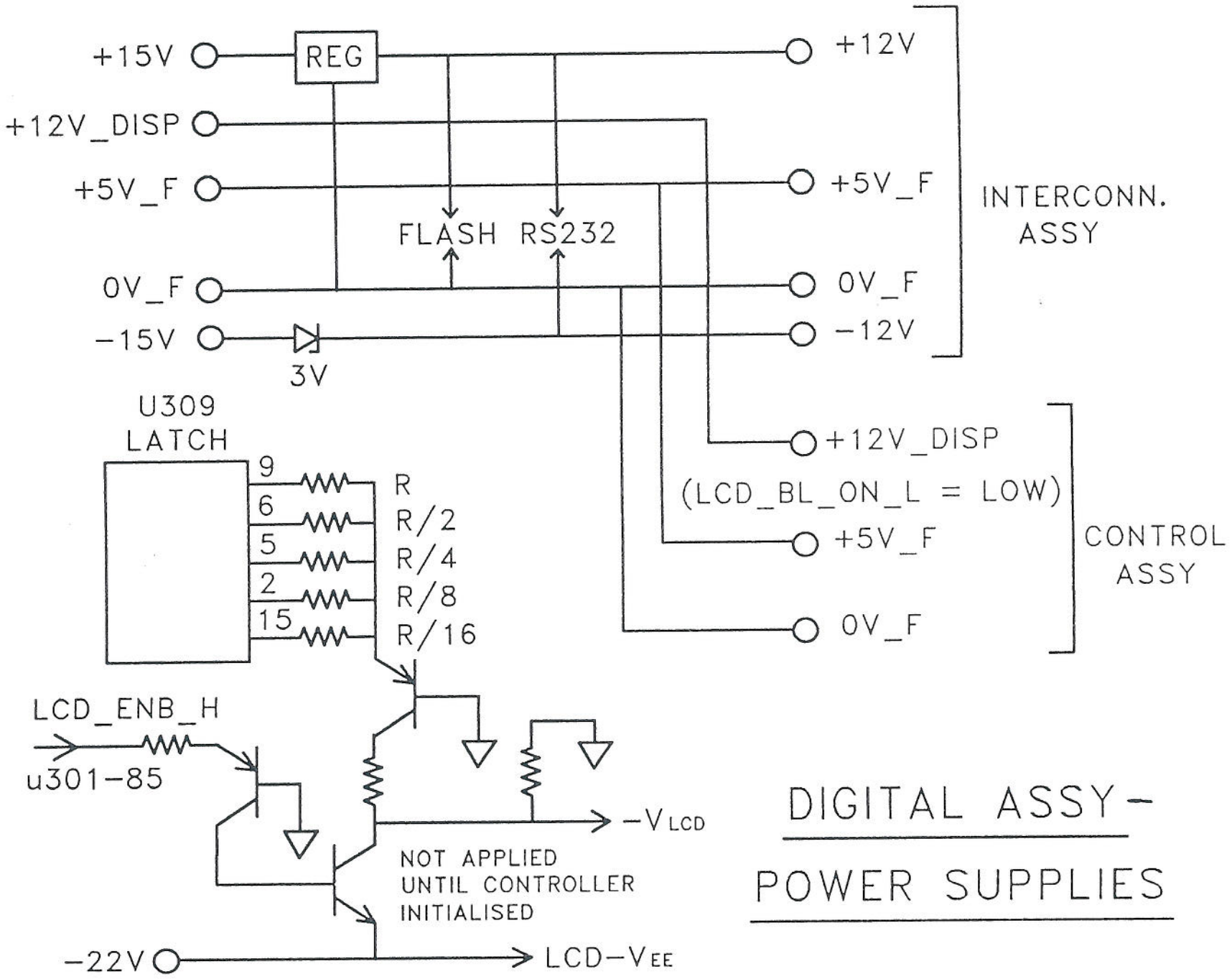
DIGITAL ASSY – PROCESSOR & MEMORY



DIGITAL ASSY – CLOCK GENERATOR, SIGNAL GENERATOR & DISPLAY ACCESS TIME–OUT

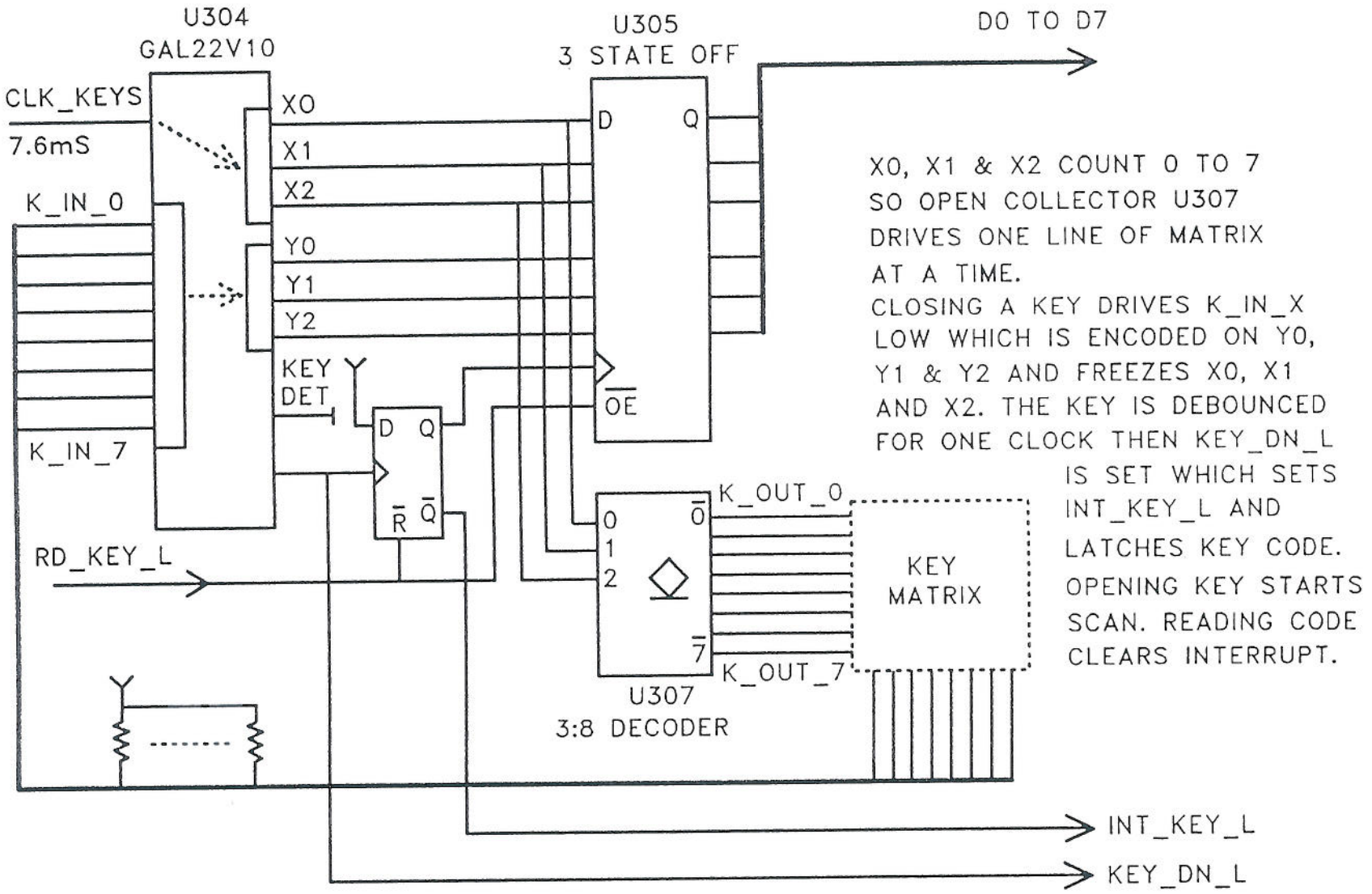


DIGITAL ASSY – LCD CONTROLLER



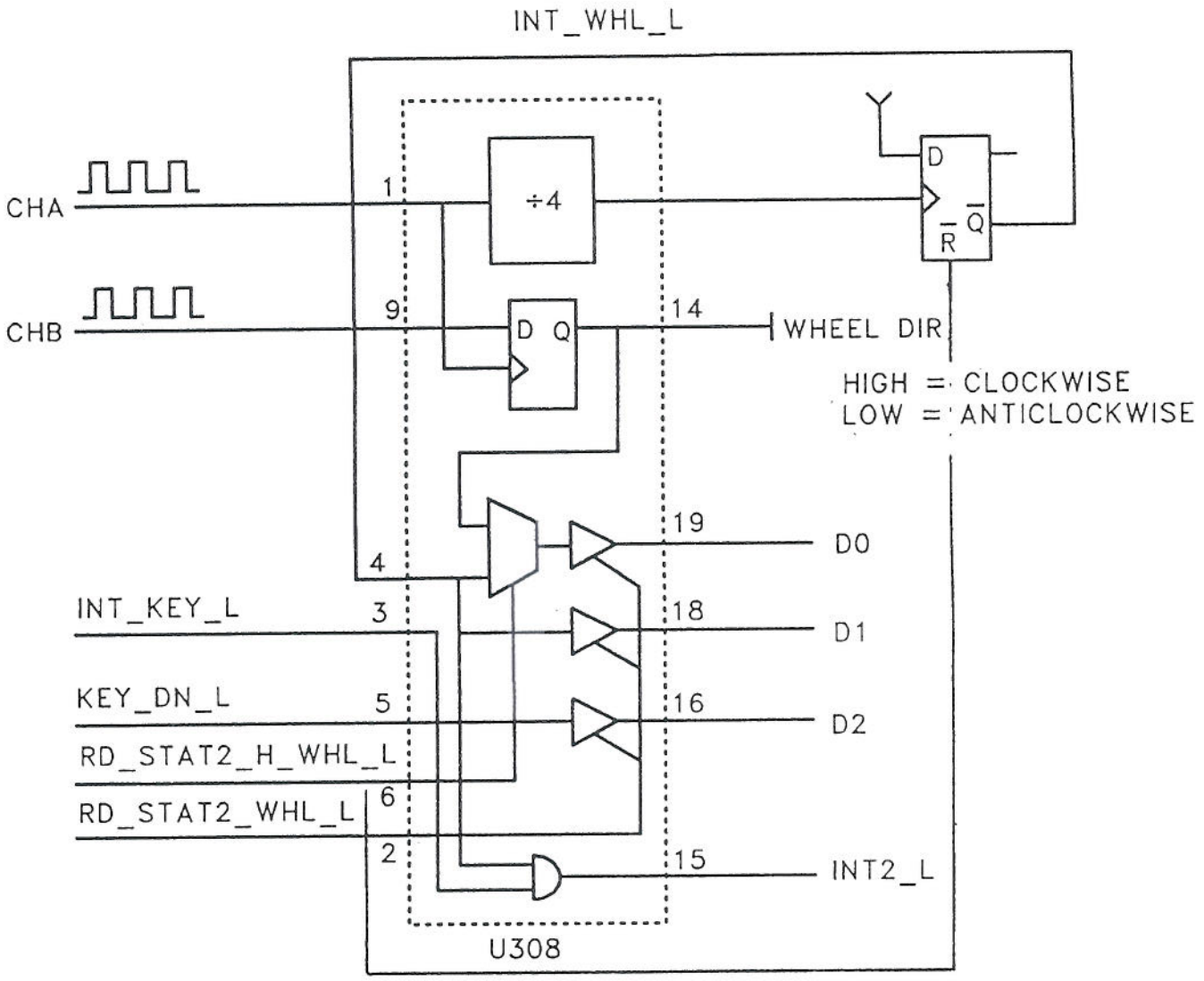
DIGITAL ASSY-

POWER SUPPLIES

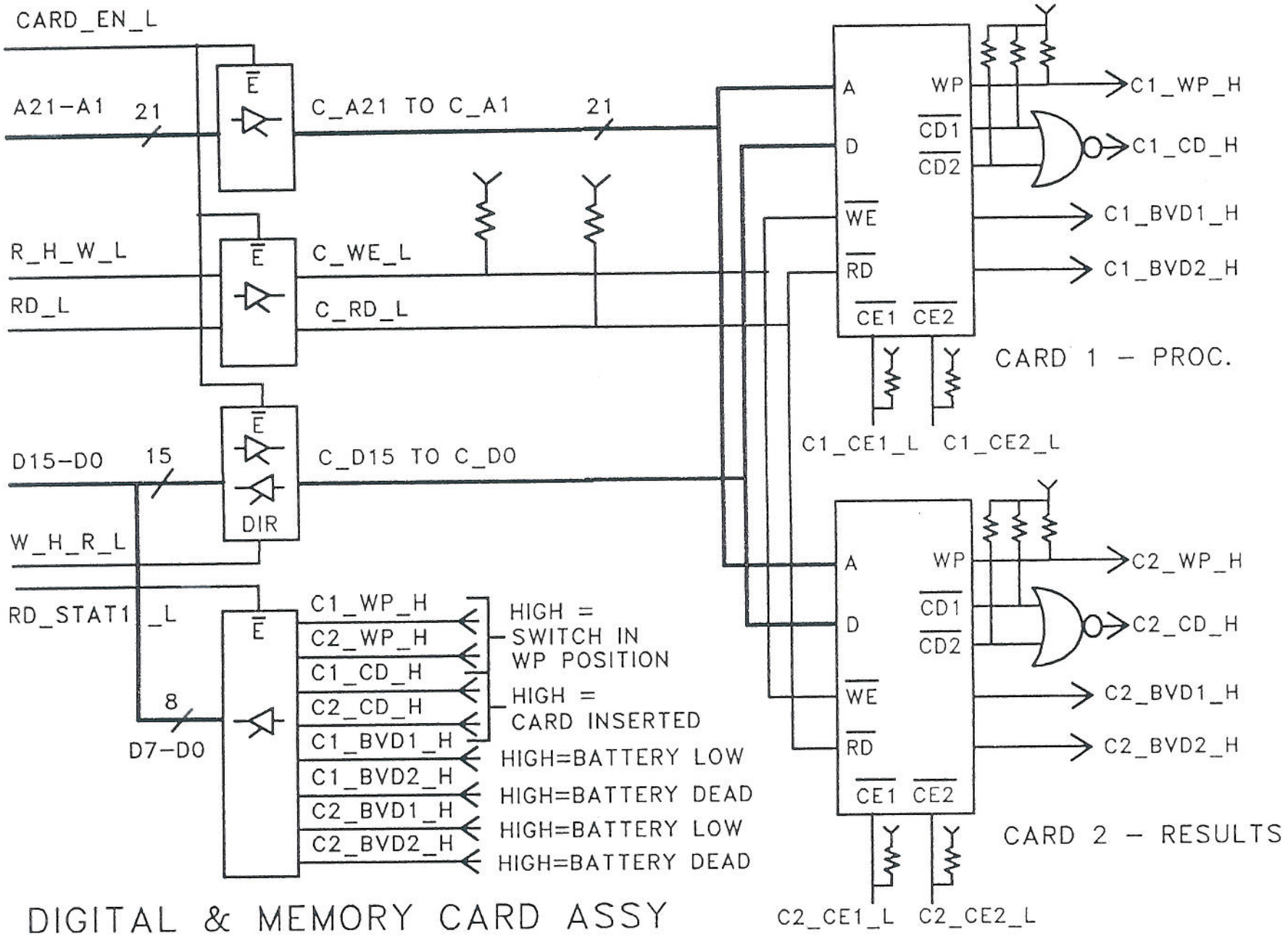


K_OUT_0 TO K_OUT_7 ALWAYS WILL APPEAR LOGIC LOW AS THEY ARE OPEN COLLECTOR.

DIGITAL ASSY – KEYBOARD ENCODER

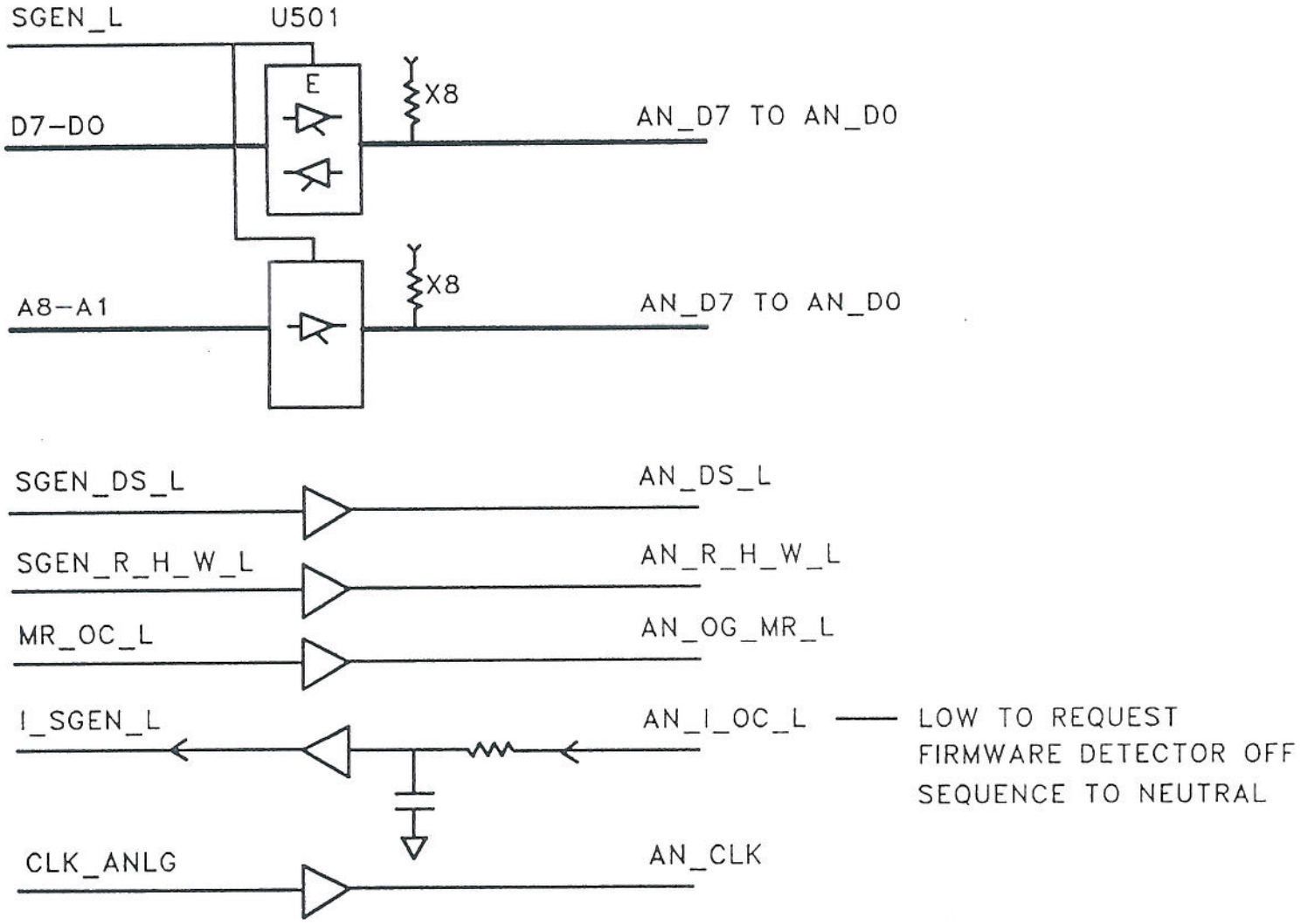


DIGITAL ASSY – ROTARY ENCODER INTERFACE & BEZEL INTERRUPTS



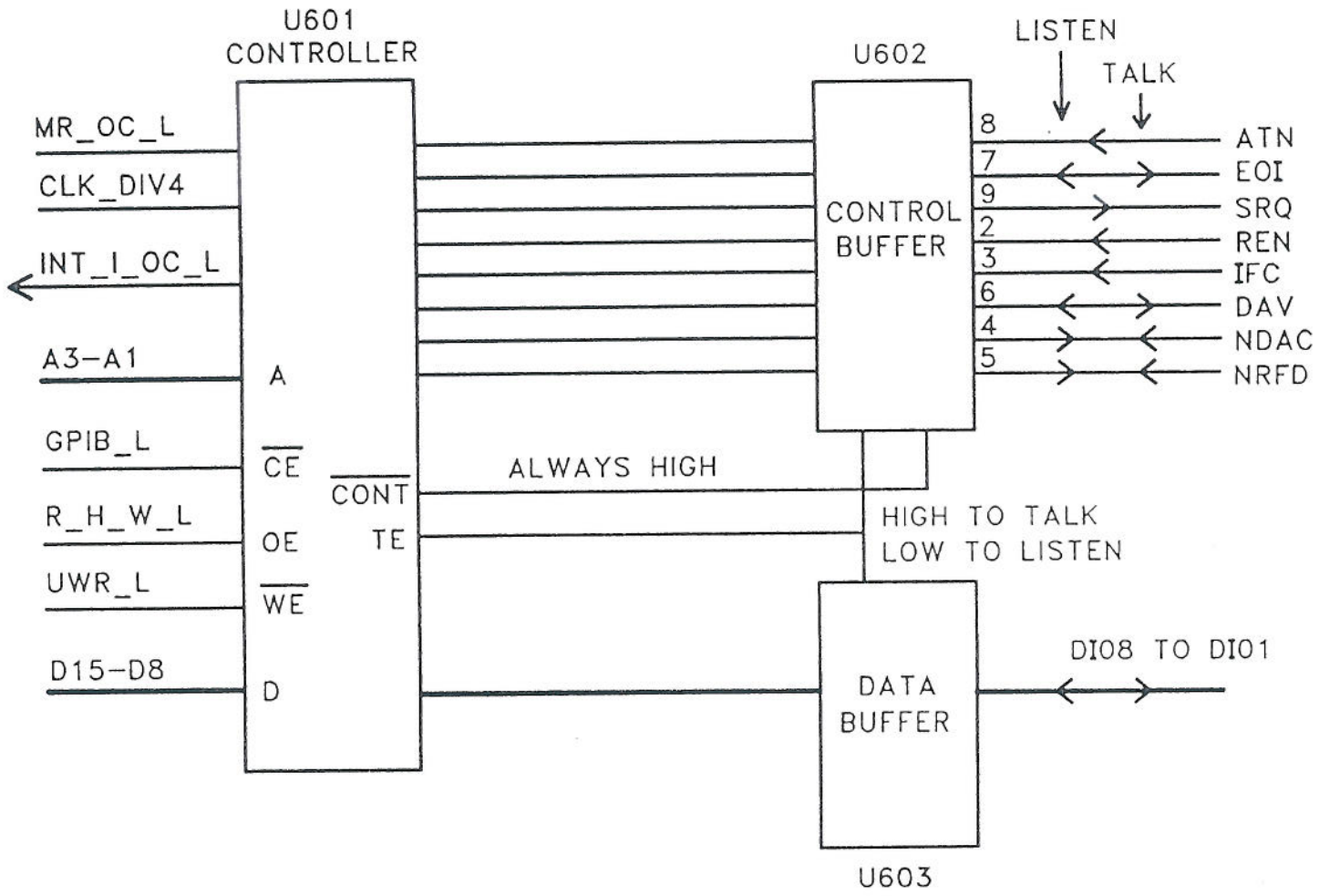
DIGITAL & MEMORY CARD ASSY

– CARD INTERFACE



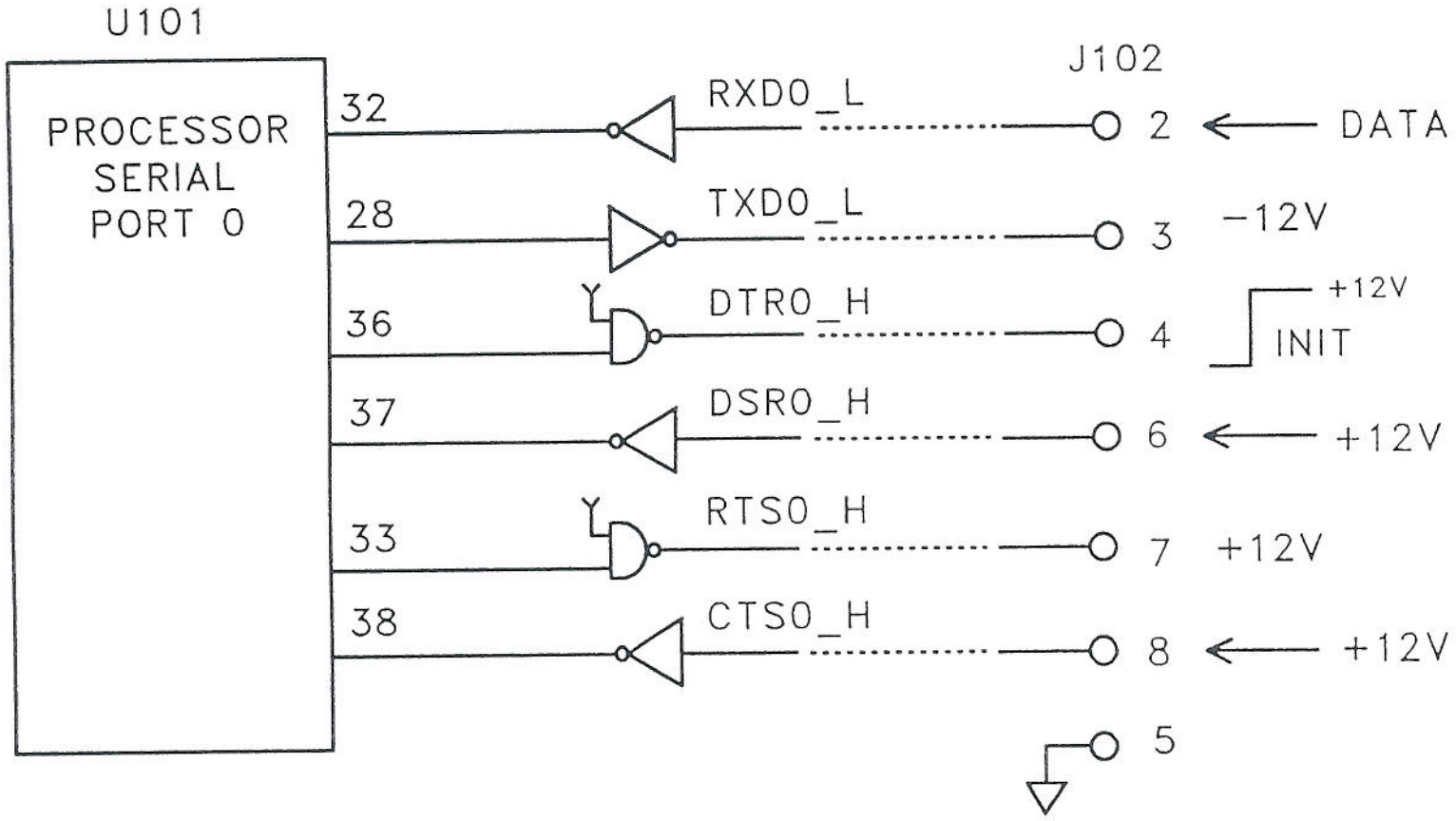
IGNORE OPTIONAL SERIAL INTERFACE ON J502.

DIGITAL ASSY – SIGNAL GENERATION PARALLEL INTERFACE



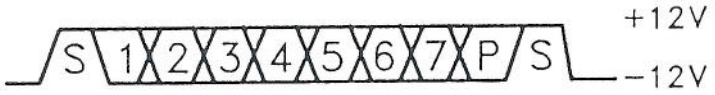
TEST BY CONNECTING A CONTROLLER AND ACCESSING ADDRESS OF 9000. CHECK PROCESSOR INTERFACE OF U601. ENSURE INT_I_OC_L IS SERVICED (GOES LOW – HIGH). BUFFER DIRECTION CONTROLLED BY TE.

DIGITAL ASSY – IEEE 488 INTERFACE



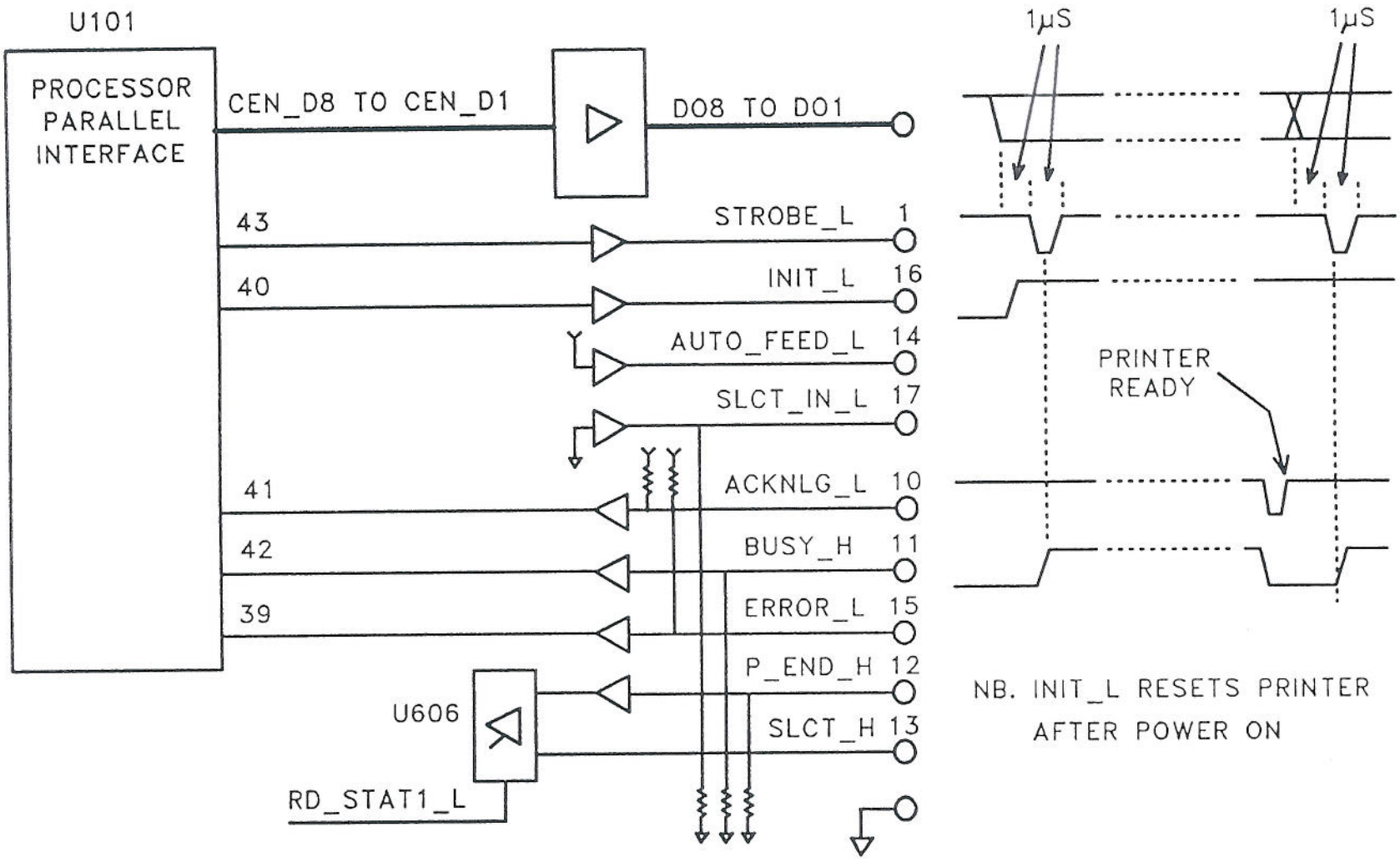
CHECK USING: MODE−TEST−INTERFACE−TRACKER.

1. ALL CONTROL IS BY UART ON PROCESSOR U101.
2. FULL MODEM CONTROL REQUIRED TO POWER TRACKER BALL FROM INTERFACE.
3. 1K2 BAUD, 7 BITS, ODD PARITY, 1 STOP BIT.



DIGITAL & INTERCONNECTION ASSY

− RS232 INTERFACE



CHECK USING: MODE–TEST–INTERFACE–PRINTER. PRODUCTION USE A TEST BOX TO SIMULATE BUSY_H=LOW (NO MESSAGE), P_EN_H=HIGH (OUT OF PAPER MESSAGE) AND ERROR_L=LOW/SLCT_H=LOW (NOT RESPONDING).

DIGITAL & INTERCONNECTION ASSY – PARALLEL PRINTER INTERFACE

1. REAR SWITCHES ARE READ BY THE FIRMWARE VIA U606 ON D15 TO D8 ENABLED BY RD_STAT1_L (D7–D0 USED FOR MEMORY CARD STATUS).

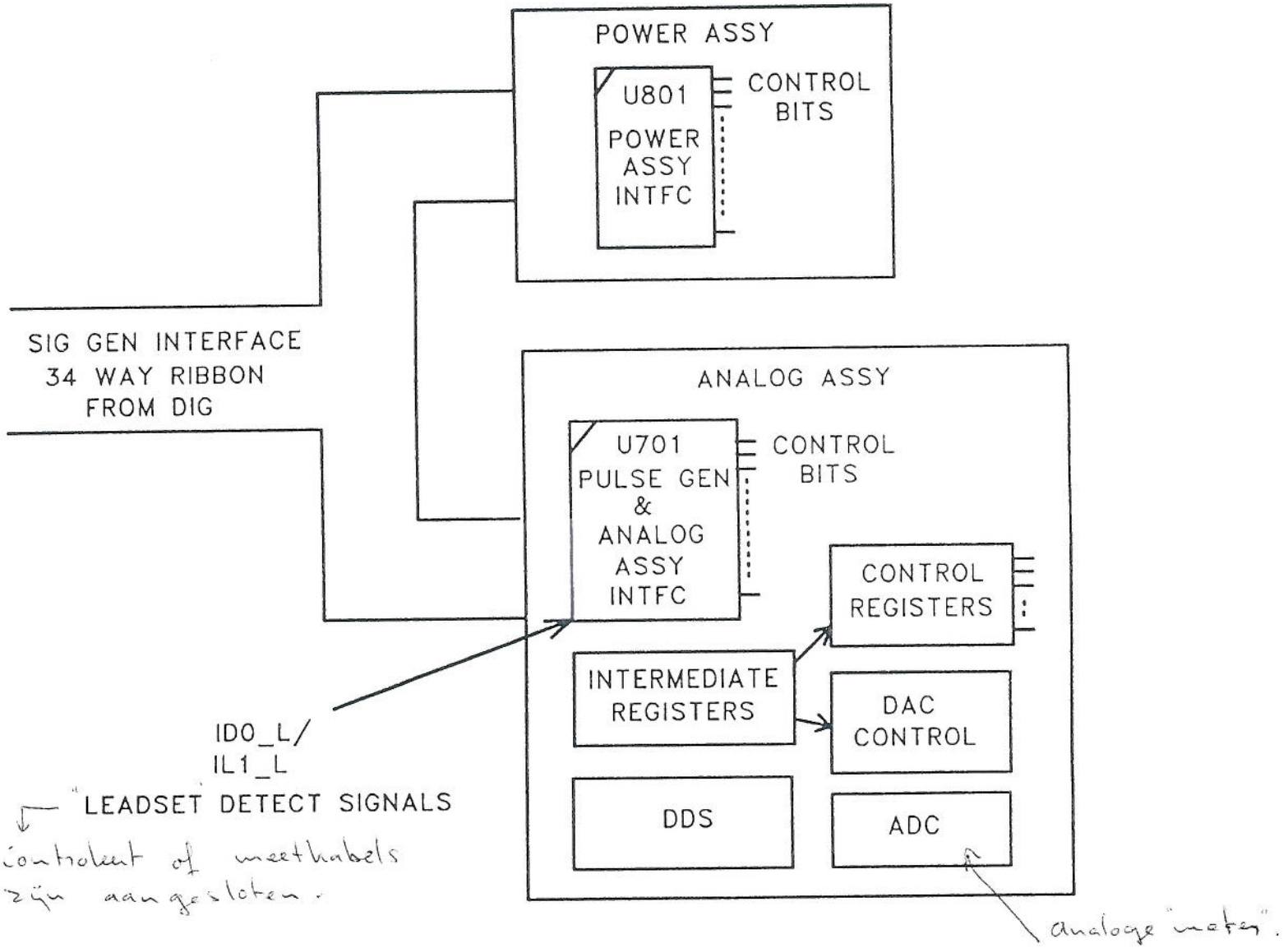
1.1 CAL_EN_L DRIVES HARDWARE PROTECTION IN U205 & U206 FOR PROM_3_L (CHAR CONST) AND PART OF EEPROM_L (CAL CONST).

1.2 BOOT_EN_L DRIVES U205 & U206 TO RECONFIGURE THE ADDRESS MAP. NORMALLY THE PROCESSOR STARTS UP AND PROM1_L WILL BE USED TO FETCH RESET VECTOR FROM FLASH. IN BOOT MODE THE FLASH (PROM1_L & PROM2_L) IS REPLACED BY C1_CE1_L/C1_CE2_L. EFFECTIVELY IT IS LOOKING FOR A RESET VECTOR AND CODE FROM THE PROCEDURE MEMORY CARD (MAX 4MBYTES). THIS ALLOWS CODE TO BE TRANSFERRED TO THE FLASH USING A MEMORY CARD HOLDING BOTH LOADER AND NEW CODE. DTACK FOR THE MEMORY CARD IS DONE BY PROCESSOR CS0 (≈380nS ON TP102). THE FLASH IS FAST VIA U702–1. THE LOADER SHOWS PROGRESS AS HORIZONTAL BARS. FIRST COLUMN ERASE U102, U103, U104, U105. SECOND COLUMN PROGRAM U102, U103, U104, U105. A CONTINUOUS TONE INDICATES FAILURE.

DIGITAL ASSY – SWITCHES & BOOT MODE

1. U701 MONITORS +5V_F SUPPLY (Vcc). KEEPS NV_EN_H LOW FOR 200mS AFTER Vcc RISES ABOVE 4.5V/4.75V. IF Vcc FALLS BELOW 4.5V/4.75V, NV_EN_H IS DRIVEN LOW IMMEDIATELY.
2. THE WATCHDOG IN U701 IS DRIVEN FROM THE FIRMWARE BY AN EDGE EVERY 64mS ON WD_TOG. IT PULSES NV_EN_H LOW FOR 200mS IF IT IS NOT SERVICED. IF NO EDGES ARE APPLIED TO WD_TOG AFTER NV_EN_H RISES THEN IT WILL BARK IN 1.6S, OTHERWISE IT WILL BE 100mS AFTER THE LAST EDGE ON WD_TOG. THIS DOES A NORMAL RESET BUT THE FIRMWARE CHECKS BARK TO TELL IF IT IS FROM POWER ON OR WATCHDOG.
3. INTENTIONALLY THE FIRMWARE MAKES THE WATCHDOG BARK TO REPORT ERRORS SUCH AS AN UNEXPECTED (OUTPUT IS OFF) POWER AMPLIFIER OVERLOAD.
4. OPEN COLLECTOR GATES DRIVE MR_OC_L & HALT_OC_L ALLOWING THE PROCESSOR TO DO A SYSTEM RESET OR INDICATE A RUNNING PROBLEM, BY DRIVING ALSO THESE SIGNALS LOW.

DIGITAL ASSY – RESET AND WATCHDOG



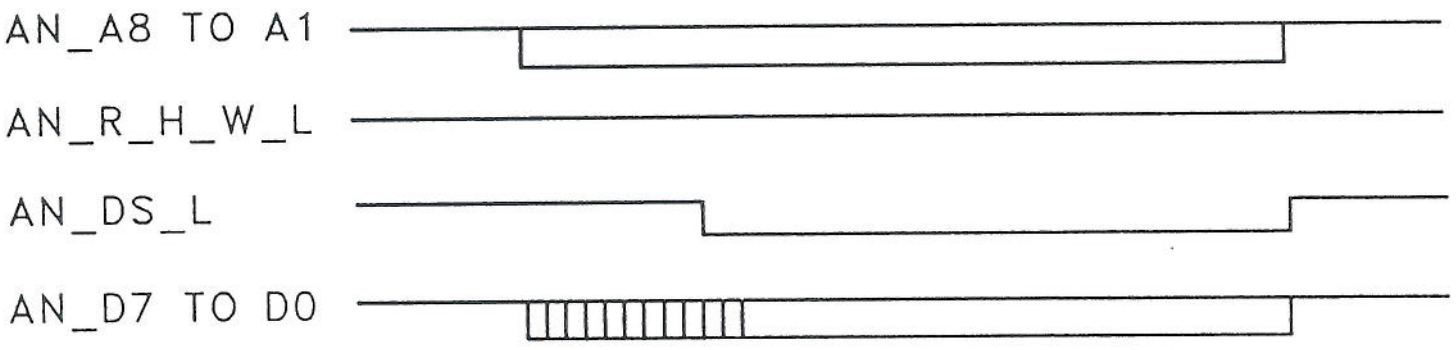
SIGNAL GENERATION CONTROL INTERFACE

1. 8 BIT DATA BUS.
2. 8 ADDRESS LINES.
3. DIRECTION & STROBE CONTROL.
4. RESET SIGNAL FROM DIGITAL ASSY.
5. CLOCK FROM DIGITAL 16mS PERIOD TO DRIVE SEQUENCING.
6. INTERRUPT FROM SIGNAL GENERATION:

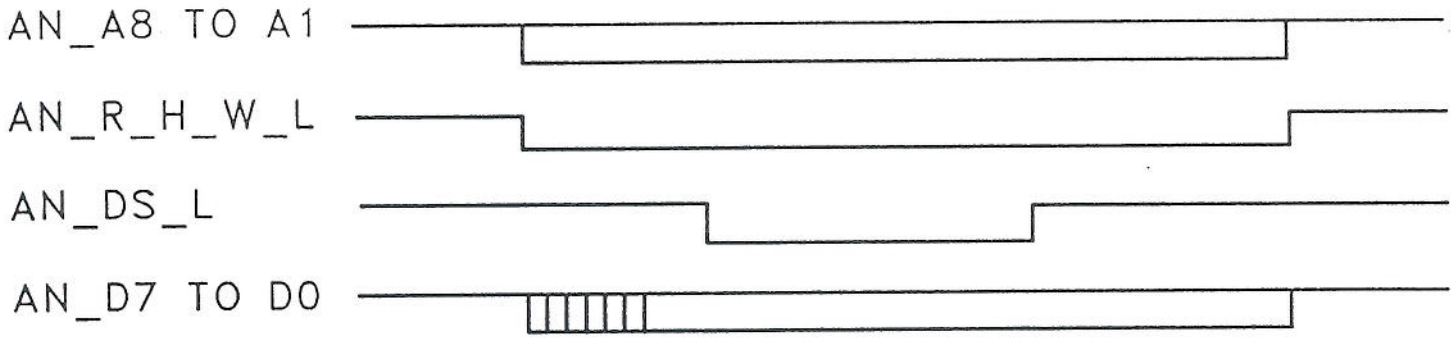
    a. OVER VOLTAGE IN CURRENT.
    b. POWER AMP OVERLOAD.
    c. HIGH VOLTAGE POWER SUPPLY OVERLOAD.
    d. OFF KEY TIME OUT.

    INTERRUPTS DISABLED BY REMOVING LINK ON ANALOG OR POWER ASSY.

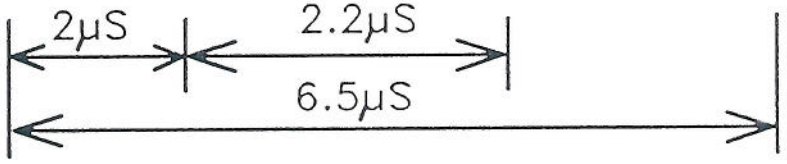
INTERFACE TO SIGNAL GENERATION CIRCUITS



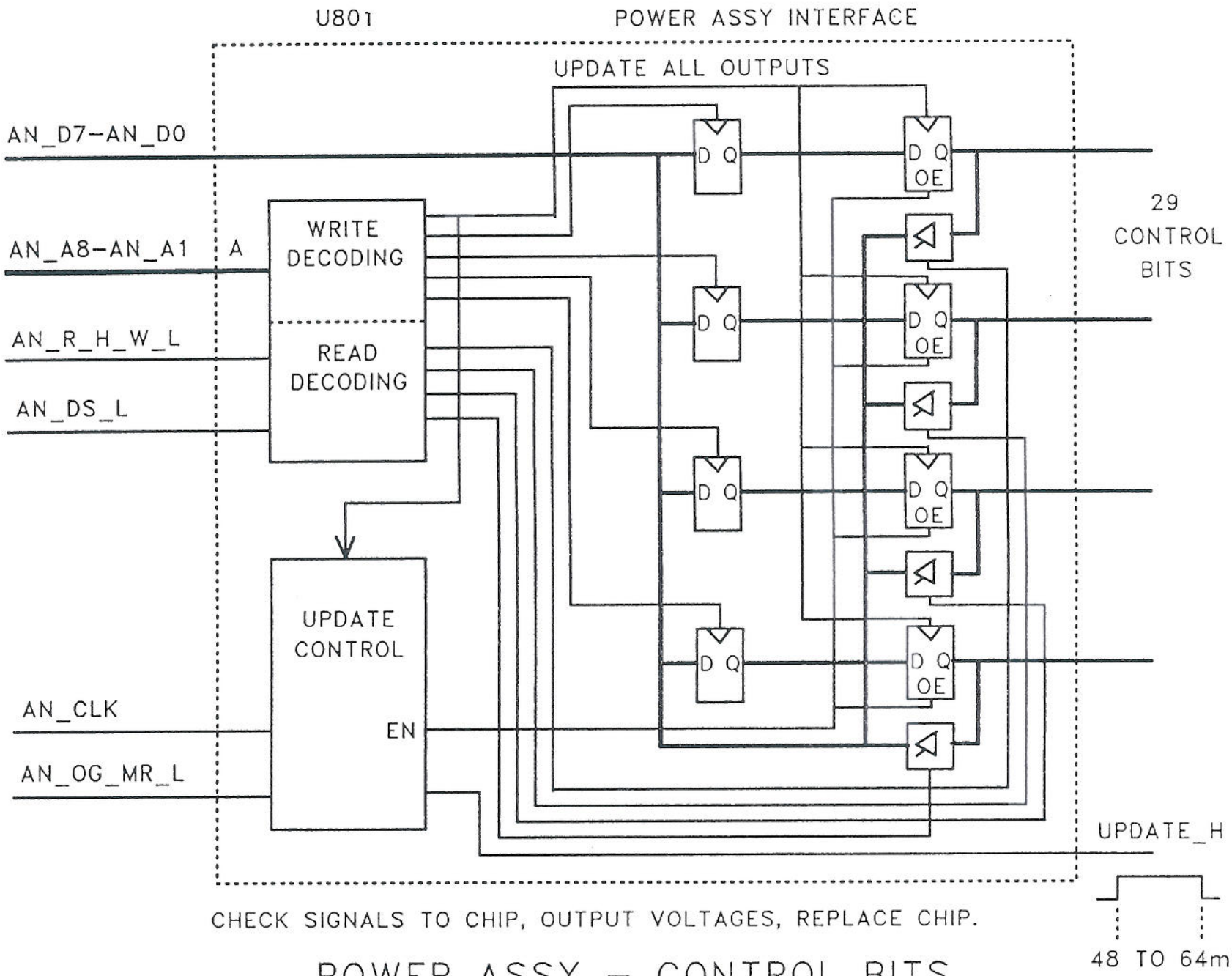
DATA FROM SIG GEN – READ



DATA TO SIG GEN – WRITE

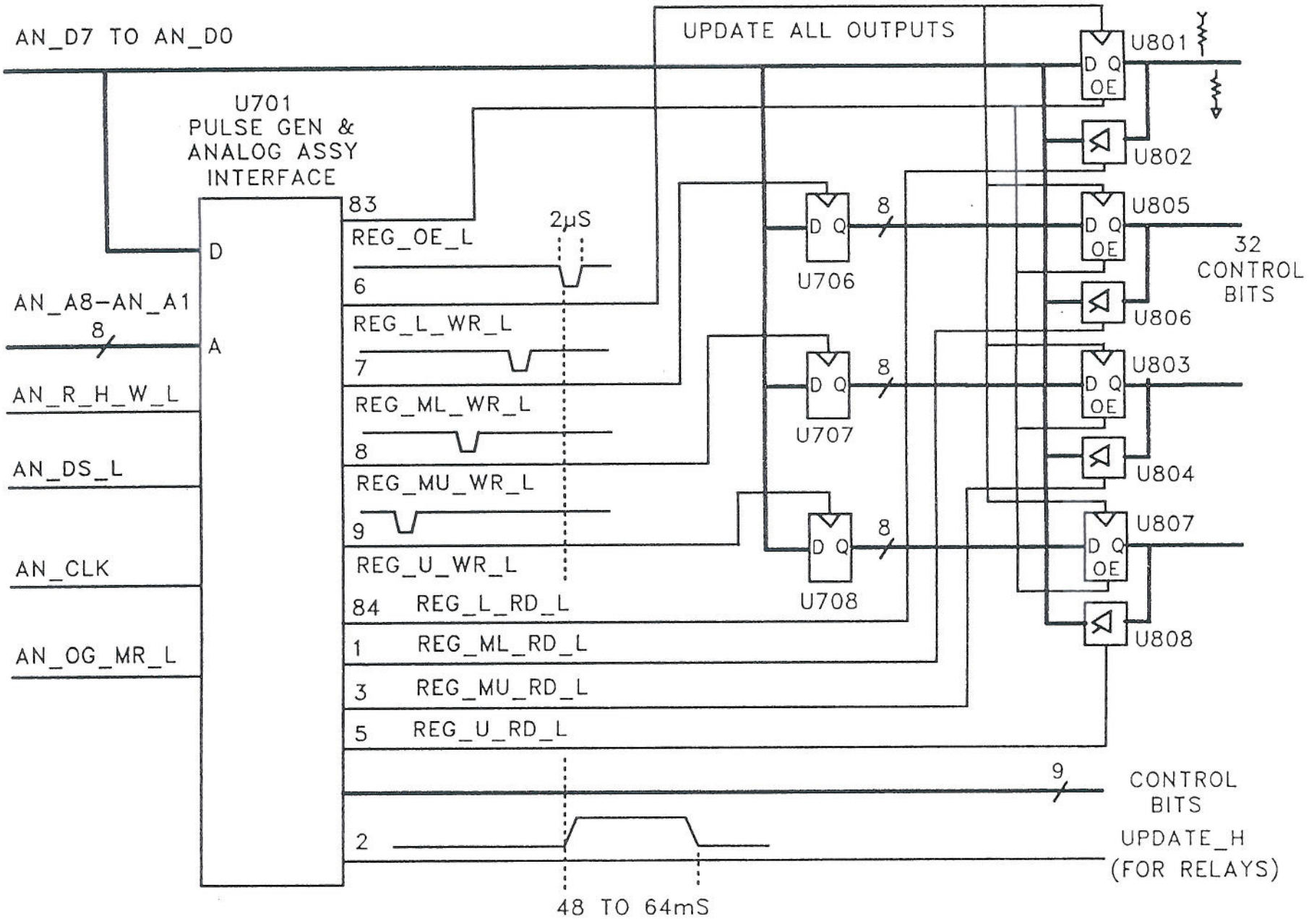


INTERFACE TO SIGNAL GENERATION CIRCUITS



POWER ASSY – CONTROL BITS

A23



ANALOG ASSY – CONTROL BITS

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